MG0018
Migration Guide

Migrating from AT32F403A/407 to AT32F435/437

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing AT32F403A/407 series to AT32F435/437 series. It brings together the most important information and lists the vital aspects that need to be taken into account.

To move an application from AT32F403A/407 series to AT32F435/437 series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F435/437xx

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1 Similarities and differences between AT32F435/437 and AT32F403A/407

AT32F435/437 series microcontrollers are not compatible with AT32F403A/407 series. AT32F435/437 series embeds additional peripherals with powerful featues and updates many peripherals with extended functions, some of which are different from AT32F403A/407, which are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, define the alternate functions of the pins.
- Compiler tools: identical, for example, Keil, IAR.

1.2 Overview of differences

Table 1. Difference summary

	AT32F435/437	AT32F403A/407
System clock	Max frequency 288 MHz, APB1 144 MHz, APB2 144 MHz	Max frequency 240 MHz, APB1 120 MHz, APB2 120 MHz
Startup	10ms(ZW = 128 KB)	13 ms
	15ms(ZW = 256 KB)	
	25ms(ZW = 512 KB)	
Wake up from Deepsleep mode (Voltage regulator is in low-power mode)	360 µs	320 µs
Wake up from Standby mode	5ms(ZW = 128 KB)	8 ms
	10ms(ZW = 256 KB)	
	20ms(ZW = 512 KB)	
SRAM size	Extended up to 512 KB	Extended up to 224 KB
Advanced timer	TMR20	-
Real-time clock	ERTC	RTC
USB	2 x USB2.0 OTG, supporing FS/LS master and FS device mode	1 x USB Device
EDMA	1	-
SDRAM	1	-
QSPI	2	-
DVP	1	-
Infrared transmitter	1	-
ADC	5.33 Msps (max ADCCLK = 80 MHz)	2 Msps (max ADCCLK = 28 MHz)
ESD	HBM: 4 KV, CDM: 1000 V	HBM: 5 KV, CDM: 1000 V
Typical current in Run mode	178.1mA@240Mhz with all peripherals enabled	100.7mA@240Mhz with all peripherals enabled

	AT32F435/437	AT32F403A/407
Typical current in Sleep mode	161.4mA@240Mhz with all peripherals enabled	85.3mA@240Mhz with all peripherals enabled
Typical current in Deepsleep mode (LDO is in low-power mode)	0.76mA	1.34mA
Typical current in Standby mode	13.51uA	6.48uA

2 Hardware migration

AT32F435/437 series is pin-to-pin compatible with AT32F403A/407 series for the same packages. As they differ in GPIO peripheral, it is necessary to refer to the corresponding Datasheet for more information on the peripheral functions of each pin.

Table 2. Peripheral compatibility analysis

AT32F435/437					AT32F403A/407				
LQFP100	LQFP64	LQFP48	QFN48	Pin name	LQFP100	LQFP64	LQFP48	QFN48	Pin name
12	5	5	5	PH0	12	5	5	5	PD0
13	6	6	6	PH1	13	6	6	6	PD1
49	31	23	23	PH3	49	31	23	23	Vss
73	47	35	35	PH2	73	47	35	35	Vss/NC

3 Boot mode compatibility

Table 3 presents the configuration of the Boot mode selection that applies to the AT32F435/437 and AT32F403A/407.

Table 3. Boot mode

Boot mode selection		Boot modes	Description
BOOT1	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	Boot memory	Boot memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

In most cases, AT32F435/437 and AT32F403A/407 series load a Boot mode on a system reset. However, for AT32F435/437 series, if embedded SRAM Boot mode is selected, the BOOT status is then locked. In this case, it is impossible to load a new Boot mode on a system reset unless a power-on reset occurs.

4 Software migration

4.1 Peripheral comparison

There are some differences between AT32F435/437 and AT32F403A/407 in terms of peripherals, some of which are new designs for AT32F435/437 series. Therefore, it is necessary to modify these peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 4. Peripheral compatibility analysis

Peripheral	AT32F435/437	AT32F403A/407	Compatibility	
			Pinout	Firmware driver
PWC	Y	Y	NA	Partial compatibility
CRM	Y	Y	Identical	Incompatible
FLASH	Y	Y	NA	Partial compatibility
GPIO	Y	Y	Identical	Incompatible
IOMUX	NA	Y	NA	Incompatible
SCFG	Y	NA	NA	Incompatible
EXINT	Y	Y	Identical	Partial compatibility
DMA	Y	Y	NA	Partial compatibility
CRC	Y	Y	NA	Full compatibility
I2C	Y	Y	Identical	Incompatible
USART	Y	Y	Identical	Partial compatibility
SPI	Y	Y	Identical	Partial compatibility
TMR	Y	Y	Identical	Partial compatibility
WWDT	Y	Y	NA	Full compatibility
WDT	Y	Y	NA	Partial compatibility
RTC	Y	Y	Identical	Incompatible
ADC	Y	Y	Identical	Incompatible
DAC	Y	Y	Identical	Partial compatibility
CAN	Y	Y	Identical	Full compatibility
OTGFS	Y	NA	NA	Incompatible
USB	NA	Y	NA	Incompatible
ACC	Y	Y	NA	Full compatibility
IRTMR	Y	NA	NA	Incompatible
XMC	Y	Y	Identical	Partial compatibility
SDIO	Y	Y	Identical	Full compatibility
QSPI	Y	NA	NA	Incompatible
DVP	Y	NA	NA	Incompatible
SDRAM	Y	NA	NA	Incompatible
EDMA	Y	NA	NA	Incompatible
DEBUG	Y	Y	NA	Incompatible

4.2 Functional differences

This section describes the peripheral differences between AT32F435/437 and AT32F403A/407. The peripheral features of the AT32F435/437 are detailed in the subsections below.

4.2.1 Memory mapping

- *Table 5* presents the differences related to address mapping and bus distribution in AT32F435/437 versus AT32F403A/407.

Table 5. Memory map differences

Peripheral	AT32F435/437		AT32F403A/407	
	Bus	Base address	Bus	Base address
SDIO2	AHB	0x50061000	AHB	0x40023400
DVP		0x50050000	N/A	N/A
OTGFS1		0x50000000	N/A	N/A
OTGFS2		0x40040000	N/A	N/A
SDIO1		0x4002C400	AHB	0x40018000
EMAC		0x40028000		0x40028000
GPIOH		0x40021C00	N/A	N/A
GPIOG		0x40021800	N/A	N/A
GPIOF		0x40021400	N/A	N/A
GPIOE		0x40021000	APB2	0x40011800
GPIOD		0x40020C00		0x40011400
GPIOC		0x40020800		0x40011000
GPIOB		0x40020400		0x40010C00
GPIOA		0x40020000		0x40010800
QSPI2	AHB1	0xA0002000	N/A	N/A
QSPI1		0xA0001000	N/A	N/A
DMA1_2		0x40026400	AHB	0x40020400
				0x40020000
EDMA		0x40026000	N/A	N/A
FLASH		0x40023C00	AHB	0x40022000
CRM		0x40023800		0x40021000
I2S3EXT	APB2	0x40017C00	APB2	0x40017000
I2S2EXT		0x40017800		0x40016C00
ACC		0x40017400		0x40015800
TMR20		0x40014C00	N/A	N/A
TMR11		0x40014800	APB2	0x40015400
TMR10		0x40014400		0x40015000
TMR9		0x40014000		0x40014C00
EXINT		0x40013C00		0x40010400
SCFG		0x40013800	N/A	N/A
SPI4		0x40013400	APB1	0x40004000
ADC1/2/3		0x40012000	APB2	0x40013C00
				0x40012800
				0x40012400
USART6		0x40011400		0x40016000
USART1		0x40011000		0x40013800
TMR8		0x40010400		0x40013400
TMR1		0x40010000		0x40012C00

Peripheral	AT32F435/437		AT32F403A/407	
	Bus	Base address	Bus	Base address
IOMUX	N/A	N/A		0x40010000
UART8	APB1	0x40007C00		0x40016800
UART7		0x40007800		0x40016400
I^2C3		0x40005C00		0x40015C00
BPR	N/A	N/A	APB1	0x40006C00
USBFS	N/A	N/A		0x40005C00
ERTC	APB1	0x40002800	N/A	N/A
RTC	N/A	N/A	APB1	0x40002800

4.2.2 CRM interface

- The main differences related to CRM (Clock and reset management) in the AT32F435/437 series versus AT32F403A/407 are as follows:
  1. PLL configuration: AT32F435/437 PLL is configured through parameters PLLCLK = (PLL reference clock * PLL_NS) / (PLL_MS * PLL_FR); AT32F403A/407 PLL is configured through fixed multiplication frequency: PLLCLK = PLL reference clock * PLL_MULT.
  2. Peripheral clock low power consumption: It is possible to disable peripheral clocks to reduce power consumption when entering Sleep mode. Each of the peripehrals of AT32F435/437 can be configured individually, while AT32F403A/407 only has SRAM and FLASH that can be configured with this feature.
  3. Clock output: AT32F435/437 supports two CLKOUT, while AT32F403A/407 has only one.
- Reference documents:

  《AN0084_AT32F435_437_CRM_Start_Guide》

  《AN0082_AT32F403A_407_CRM_Start_Guide》

4.2.3 Flash interface

- The Flash memory differences between AT32F435/437 and AT32F403A/407 are shown in *Table 6* .

Table 6. Flash memory differences

Position	AT32F435/437	AT32F403A/407
Boot memory	0x1FFF0000-0x1FFF3FFF	0x1FFFB000-0x1FFFEFFF
User System Data area	0x1FFFC000-0x1FFFC1FF	0x1FFFF800-0x1FFFF82F

4.2.4 SRAM interface

- AT32F403A/407 SRMA is a whole, while the AT32F435/437 SRAM can be as a whole, or split into two parts, SRAM1 and SRAM2.
- Reference documents:

  《AN0092_AT32F435_437_Performance_Improve》

4.2.5 Interrupt vectors

- *Table 7* presents the interrupt vector differences in AT32F435/437 series versus AT32F403A/407 series.

Table 7. Interrupt vector differences

Position	AT32F435/437	AT32F403A/407
0	WWDT	WWDT
1	PVM	PVM
2	TAMPER	TAMPER
3	ERTC	RTC
4	FLASH	FLASH
5	CRM	CRM
6	EXINT0	EXINT0
7	EXINT1	EXINT1
8	EXINT2	EXINT2
9	EXINT3	EXINT3
10	EXINT4	EXINT4
11	EDMA_Stream1	DMA1_CH1
12	EDMA_Stream 2	DMA1_CH2
13	EDMA_Stream 3	DMA1_CH3
14	EDMA_Stream 4	DMA1_CH4
15	EDMA_Stream 5	DMA1_CH5
16	EDMA_Stream 6	DMA1_CH6
17	EDMA_Stream 7	DMA1_CH7
18	ADC1_2_3	ADC1_2
19	CAN1_TX	USBFS_H_CAN1_TX
20	CAN1_RX0	USBFS_L_CAN1_RX0
21	CAN1_RX1	CAN1_RX1
22	CAN_SE	CAN1_SE
23	EXINT9_5	EXINT9_5
24	TMR1_BRK_TMR9	TMR1_BRK_TMR9
25	TMR1_OVF_TMR10	TMR1_OVF_TMR10
26	TMR1_TRG_HALL_TMR11	TMR1_TRG_HALL_TMR11
27	TMR1_CH	TMR1_CH
28	TMR2	TMR2
29	TMR3	TMR3
30	TMR4	TMR4
31	I2C1_EVT	I2C1_EVT
32	I2C1_ERR	I2C1_ERR
33	I2C2_EVT	I2C2_EVT
34	I2C2_ERR	I2C2_ERR
35	SPI1	SPI1
36	SPI2_I2S2EXT	SPI2_I2S2EXT
37	USART1	USART1
38	USART2	USART2
39	USART3	USART3
40	EXINT15_10	EXINT15_10
41	ERTCAlarm	RTCAlarm
42	OTGFS1_WKUP	USBFS_WKUP

Position	AT32F435/437	AT32F403A/407
43	TMR8_BRK_TMR12	TMR8_BRK_TMR12
44	TMR8_OVF_TMR13	TMR8_OVF_TMR13
45	TMR8_TRG_HALL_TMR14	TMR8_TRG_HALL_TMR14
46	TMR8_CH	TMR8_CH
47	EDMA_Stream 8	ADC3
48	XMC	XMC
49	SDIO1	SDIO1
50	TMR5	TMR5
51	SPI3_I2S3EXT	SPI3_I2S3EXT
52	UART4	UART4
53	UART5	UART5
54	TMR6_DAC	TMR6
55	TMR7	TMR7
56	DMA1_CH1	DMA2_CH1
57	DMA1_CH2	DMA2_CH2
58	DMA1_CH3	DMA2_CH3
59	DMA1_CH4	DMA2_CH5_4
60	DMA1_CH5	SDIO2
61	EMAC	I2C3_EVT
62	EMAC_WKUP	I2C3_ERR
63	CAN2_TX	SPI4
64	CAN2_RX0	Reserved
65	CAN2_RX1	Reserved
66	CAN2_SE	Reserved
67	OTGFS1	Reserved
68	DMA1_CH6	CAN2_TX
69	DMA1_CH7	CAN2_RX0
70	Reserved	CAN2_RX1
71	USART6	CAN2_SE
72	I2C3_EVT	ACC
73	I2C3_ERR	USBFS_MAPH
74	Reserved	USBFS_MAPL
75	Reserved	DMA2_CH7_6
76	OTGFS2_WKUP	USART6
77	OTGFS2	UART7
78	DVP	UART8
79	Reserved	EMAC
80	Reserved	EMAC_WKUP
81	FPU	Reserved
82	UART7	Reserved
83	UART8	Reserved
84	SPI4	Reserved
85	Reserved	Reserved
86	Reserved	Reserved

Position	AT32F435/437	AT32F403A/407
87	Reserved	Reserved
88	Reserved	Reserved
89	Reserved	Reserved
90	Reserved	Reserved
91	QSPI2	Reserved
92	QSPI1	Reserved
93	Reserved	Reserved
94	Reserved	Reserved
95	Reserved	Reserved
96	Reserved	Reserved
97	Reserved	Reserved
98	Reserved	Reserved
99	Reserved	Reserved
100	Reserved	Reserved
101	Reserved	Reserved
102	SDIO2	Reserved
103	ACC	Reserved
104	TMR20_BRK	Reserved
105	TMR20_OVF	Reserved
106	TMR20_TRG_HALL	Reserved
107	TMR20_CH	Reserved
108	DMA2_CH1	Reserved
109	DMA2_CH2	Reserved
110	DMA2_CH3	Reserved
111	DMA2_CH4	Reserved
112	DMA2_CH5	Reserved
113	DMA2_CH6	Reserved
114	DMA2_CH7	Reserved

4.2.6 DMA interface

- There are some differences related to DMA between AT32F435/437 and AT32F403A/407, including:
  1. AT32F435/437 supports DMA and EDMA, while AT32F403A/407 supports DMA only.
  2. AT32F435/437 series supports DMA flexible mapping mode, while the AT32F403A/407 series contain two DMA mapping mode, fixed mapping and flexible ones.
- Reference documents:

  《AN0090_AT32F435_437_EDMA_Application_Note》

  《AN0103_AT32F435_437_DMA_Application_Note》

4.2.7 PWC interface

Table 8. PWC interface differences

PWC	AT32F435/437	AT32F403A/407
Wake-up pin from Standby mode	2 x wake-up Pin	1 x wake-up Pin
LDO	Programmble LDO	Not support

- *Table 8* presents the differences between the PWR interface of the AT32F435/437 series and AT32F403A/407 series. The AT32F435/437 series adds one more wake-up pin (SWPEN2-PC13) from Standby mode in order to adapt to more application scenarios, compared to AT32F403A/407. In addition, AT32F435/437 adds a LDO regulation feature to regulate the LDO voltage output freely. For more information, refer to the corresponding data sheet.

4.2.8 ADC interface

- *Table 9* presents the differences related to ADC peripheral between AT32F435/437 and AT32F403A/407. They are incompatible in software.

Table 9. ADC interface differences

ADC	AT32F435	AT32F403A
Number of channels	24 external channels + 3 internal channels (additional V_{BAT}/4)	16 external channels + 2 internal channels
Resolution	12/10/8/6-bit programmable	12-bit
Oversampling	2 to 256 times hardware oversampling	Not support
Sampling rate	Up to 5.33MSPS	2MSPS
Trigger edge	Rising/falling/both edges	Rising edge only
Trigger source	Each regular/preempted group has its respective 30 trigger sources	Each regular/preempted group has its respective 11 trigger sources
End of conversion	ADC sequence conversion can be stopped in transition	Not support
Overflow detection	Support overflow detection, with correspondi ng flag bits and interrupts	Not support
Master/slave mode	Support single slave mode (ADC1+ADC2) and dual slave mode (ADC1+ADC2+ADC3)	Support single slave mode only (ADC1+ADC2)
Data acquisition	Support CPU read and DMA read; DMA flexible mapping mode only, see DMA interface for details	Support CPU read and DMA read DMA fixed mapping mode only, refer to DMA interface for details.

- Reference documents:

  《AN0093_AT32F435_437_ADC_Application_Note》

4.2.9 EXINT interface

- There are some differences between the external interrupt configuration mode of the AT32F435/437 series and AT32F403A/407 series. The AT32F403A/407 series uses the IOMUX_EXINTCx register to configure external interrupts, while AT32F435/437 series uses the SYSCFG_EXTICRx register. In this way, only the mapping address of the EXTICRx register has changed, without any change to the meaning of EXTIx configuration

4.2.10 GPIO interface

- The differences related to GPIO peripheral in the AT32F435/437 series versus AT32F403A/407 series are described as follows:

  AT32F435/437:

  AT32F435/437 series GPIOs are configured through three registers, GPIOx_CFGR register (configure IO operating mode), GPIOx_OMODE register (configure output mode) and GPIOx_PULL register (configure IO pull-up/pull-down). The IO pull-up/pull-down configurations apply to the general-purpose input/output mode and alternate function mode.

  AT32F403A/407:

  AT32F403A/407 series GPIOs are configured through two registers, GPIOx_CFGLR and GPIOx_CFGHR. These registers can be used to configure IO operating mode, output mode and IO pull-up/pull-down mode. The IO pull-up/pull-down configurations apply to the input mode.

- Reference documents:

  《AN0096_AT32F435_437_GPIO_Application_Note》

4.2.11 IOMUX

- The differences related to IOMUX peripheral in the AT32F435/437 series versus AT32F403A/407 series are described as follows:

  AT32F435/437:

  For AT32F435/437 series, it is required that the I/O pin is configured as alternate function for peripherals to use I/O functions properly.

  Pin multiplexing and mapping are configured through the GPIOx_MUXL and GPIOx_MUXH registers.

  AT32F403A/407:

  I/O alternate function configuration depends on the peripheral mode used. For instance, the USART Tx pin should be configured as alternate function push-pull, and the USART Rx should be input floating or input pull-up.

  To optimize the number of peripheral I/O functions on different packages, it is possible to remap some alternate functions to other pins. The IOMUX_REMAPx register is used to configure the alternate functions of the peripheral pins.

- Reference documents:

  《AN0096_AT32F435_437_GPIO_Application_Note》

4.2.12 SPI interface

- In addition to the original SPI features, AT32F435/437 series has additional features compared to AT32F403A/407 series:

  1. Frequency division by 3

  This feature is enabled by setting the MDIV3EN bit within the CTRL2 register.

  2. TI mode

  This mode is enabled by setting the TIEN bit within the CTRL2 register. (Refer to Section 13.2.7 of the AT32F435/437 series Reference Manual)

4.2.13 I²C interface

- AT32F435/437 series I2C peripheral is different from that of AT32F403A/407 series. They are incompatible in software.
- Reference documents:

  《AN0091_AT32F435_437_I2C_Application_Note》

4.2.14 USART interface

- Apart from retaining all USART features of AT32F403A/407), AT32F435/437 series also provides TX/RX SWAP function (enabled through the SWAP bit, refer to Section 12.9 of the AT32F435/437 series Reference Manaul), and RS485 communication mode.

4.2.15 Security library interface

- The security library of the AT32F435/437 series is optimized compared to the AT32F403A/407. They are incompatible in software.
- Reference documents:

  《AN0040_AT32F403A_407_Security_Library_Application_Note》

  《AN0081_AT32F435_437_Security_Library_Application_Note》

4.2.16 Real-time clock interface

- AT32F435/437 embeds an ERTC feature (enhanced RTC), incompatible with the RTC of AT32F403A/407.
- Reference documents:

  《AN0047_AT32_ERTC_Application_Note》

4.2.17 WDT interface

- AT32F435/437 WDT peripheral adds a window feature. All other features are the same except the window feature. Software is compatible. AT32F435/437 is downward compatible with AT32F403A/407.

4.2.18 OTGFS interface

- AT32F435/437 supprts two OTGFS modules. Master supports USB 2.0 full speed and low speed, while the device supports USB 2.0 full speed.
- AT32F403A/407 supports USB 2.0 full speed device.
- Reference documents:

  《AN0098_AT32F435_437_OTGFS_Application_Note》

  《AN0097_AT32_MCU_USB_Device_Library_Application_Note》

  《AN0094_AT32_MCU_USB_Host_Library_Application_Note》

4.2.19 EMAC interface

- AT32F437 EMAC interface is fully compatible with AT32F407 EMAC.

4.2.20 CAN interface

- The filtering banks of the AT32F435/437 CAN peripheral are increased from 14 (for AT32F403A/407) to 28, without any change to other features. Software is compatible. AT32F435/437 is downward compatible with AT32F403A/407.

4.2.21 DAC interface

- The DAC peripheral of the AT32F435/437 adds DMA underflow detection feature compared to AT32F403A/407. It also includes DAC_STS register to store DMA underflow flag, and DAC underflow error interrupt enable bit and interrupt vectors, without any change to other features. Software is compatible. AT32F435/437 is downward compatible with AT32F403A/407.

4.2.22 TMR interface

- In TMR peripheral, AT32F435/437 adds the description of the channel 5 of advanced timers (TMR1, TMR8 and TMR20), including two registers of TMRx_CM3 and TMRx_C5DT, channel interrupt, flag and other bits
- In TMR peripheral, AT32F435/437 supports TRGOUT2 output feature for advanced timers (TMR1, TMR8 and TMR20). This feature is enabled through the TRGOUT2EN bit in the TMRx_CTRL2 register
- In AT32F435/437, the repetition period register (TMRx_RPR) of advanced timers (TMR1, TMR8 and TMR20) is expanded to be 16-bit registers.

4.3 Functional enhancement

This section describes the enhanced peripheral features in the AT32F435/437 series compared to AT32F403A/407, detailed in the subsections below.

4.3.1 AT32F435/437 additional WKUP pins

- Apart from retaining the original WKUP pin (WKUP1-PA0) used in AT32F403A/407, the AT32F435/437 series adds one more WKUP pin from Standby mode.

  WKUP pin 1——PA0

  WKUP pin 2——PC13

  Both WKUP pins have their respective enable bits (Refer to Section 2.4.2 of the AT32F435/437 series Reference Manual). When enabled, the wake-up event on the corresponding pin can wake up from Standby mode. It is possible to enable one or more wake-ups pins to wake up from Standby mode according to the actual application requirements.

4.3.2 AT32F435/437 additional TMR20 timer

- AT32F435/437 embeds an advanced timer TMR20, which cover all features of TMR1 or TMR8.
- Reference documents:

  《AN0085_AT32_MCU_TMR_Start_Guide》

4.3.3 AT32F435/437 infrared transmitter

- This infrared transmitter is based on the internal connection between TMR10 and USART1, or USART2 and TMR11. The TMR11 is used to provide carrier frequency, while the TMR10, USART1 or USART2 provides the main signals to be sent. The infrared output signal is available on PB9 or PA13.

4.3.4 AT32F435/437 additional DVP interface

- AT32F435/437 embeds a digital camera interface, which can be connected to a digital camera module through an 8~14-bit parallel interface in order to receive video data. This camera interface supports up to 54 MB/s data rate at 54 MHz.
- Reference documents:

  《AN0087_AT32_MCU_DVP_Application_Note》

4.3.5 AT32F435/437 additional QSPI interface

- AT32F435/437 adds a QSPI interface. This interface can use 4-wire mode communication or access to memories, and support XIP feature.
- Reference documents:

  《AN0088_AT32_MCU_QSPI_Application_Note》

4.3.6 AT32F435/437/437 additional SDRAM interface

- AT32F435/437 adds a SDRAM interface to support 8-bit or 16-bit SDRAM device.
- Reference documents:

  《AN0089_AT32_MCU_SDRAM_Application_Note》

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
2021.10.18	2.0.0	Initial release
2022.02.28	2.0.1	Update the document format.
2022.08.18	2.0.2	Updated the description of “data acquisition” in *Table 9*
2022.10.19	2.0.3	Added *4.2.22 TMR interface*

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