MG0017

Migration Guide

Migrating from AT32F415 to AT32F421

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing AT32F415 series to AT32F421 series. It brings together the most important information and lists the vital aspects that need to be taken into account.

To move an application from AT32F415 series to AT32F421 series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F421xx

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1 Similarities and differences between AT32F421 and AT32F415

AT32F421 series microcontrollers are basically compatible with the AT32F415 series, and provide many enhanced features, some of which are different from AT32F415. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, define the alternate functions of the pins.
- Compiler tools: identical, for example, Keil, IAR.

1.2 Overview of differences

Table 1. Differences between AT32F421 and AT32F415

	AT32F421	AT32F415
System clock	Max frequency 120 MHz, APB1 120 MHz, APB2 120 MHz	Max frequency 150 MHz, APB1 75 MHz, APB2 75 MHz
Startup	4.5 ms	600 µs
Wake up from low-power mode (Voltage regular is in low-power mode)	450 µs	360 µs
Wake up from Standby mode	1250 µs	600 µs
SRAM size	8/16 KB by part number	Fixed 32 KB
General-purpose timer	5 x timers, TMR15~17 has complementary output timers	8 x timers
Basic timer	TMR6	-
Backup register	5 x 32-bit backup registers	20 x 32-bit backup registers
CAN interface	N/A	1
USB	N/A	1 x USB2.0 OTG, supporting FS/LS master and FS device modes
Comparator	1 x COMP 4-level speed/power consumption selection, with blanking output function	2 x COMPs 2-level speed/power consumption selection
USART	TX/RX SWAP feature	-
Infrared transmitter	1	-
Power consumption at Shut-down mode	210 uA (Voltage regulator is in low-power mode)	680 uA (Voltage regulator is in low-power mode)

2 Hardware migration

AT32F421 series is pin-to-pin compatible with AT32F415 series, except for the GPIO port multiplexed as HEXT. All peripherals share the same pins in the two devices, with the only difference that AT32F421 embeds one CMP while the AT32F415 embeds two CMPs due to their peripheral difference, meaning that they differ on the alternate functions of the pins. Refer to the corresponding datasheet for more information on the pins.

Table 2. Peripheral compatibility analysis

AT32F421	AT32F415
PF0	PD0
PF1	PD1

3 Boot mode compatibility

Table 3 presents the configurations of the Boot mode selection for AT32F421 and AT32F415.

Table 3. Boot modes

Boot mode selection		Boot modes	Description
BOOT1	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	Boot memory	Boot memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

- For AT32F415 series, BOOT0 corresponds to the BOOT0 pin, and BOOT1 to PB2 pin, and the Boot mode is determined by the level of the peripheral circuitry of the corresponding pin.
- For AT32F421 series, BOOT0 corresponds to the BOOT0 pin, and BOOT1 to the nBOOT1 bit of the user option bytes (nBOOT1 default value 1 corresponds to the BOOT1 status value 0). The Boot mode is determined by the peripheral circuitry level of the BOOT0 pin and the user option bytes nBOOT1 bit value.

4 Software migration

4.1 Peripheral comparison

The differences related to the address map and bus distribution between AT32F421 and AT32F415 are shown in *Table 4*.

Table 4. Peripheral compatibility analysis

Peripheral	AT32F415		AT32F421	
	Bus	Base address	Bus	Base address
USBOTG	AHB	0x50000000	N/A	N/A
CRC		0x40023000	AHB	0x40023000
FLASH		0x40022000		0x40022000
CRM		0x40021000		0x40021000
DMA2		0x40020400	N/A	N/A
DMA		0x40020000	AHB	0x40020000
GPIOF		0x4001C000		0x48001400
GPIOD		0x40014000	N/A	N/A
GPIOC		0x40011000	AHB	0x48000800
GPIOB		0x40010C00		0x48000400
GPIOA		0x40010800		0x48000000
SDIO		0x40018000	N/A	N/A
ACC	APB2	0x40015800	N/A	N/A
TMR11		0x40015400	N/A	N/A
TMR10		0x40015000	N/A	N/A
TMR9		0x40014C00	N/A	N/A
TMR17		0x40014800	APB2	0x40014800
TMR16		0x40014400		0x40014400
TMR15		0x40014000		0x40014000
USART1		0x40013800		0x40013800

Peripheral	AT32F415		AT32F421	
	Bus	Base address	Bus	Base address
SPI1		0x40013000		0x40013000
TMR1		0x40012C00		0x40012C00
ADC		0x40012400		0x40012400
EXINT		0x40010400		0x40010400
SCFG	N/A	N/A		0x40010000
IOMUX	APB2	0x40010000	N/A	N/A
PWC		0x40007000	APB1	0x40007000
CAN		0x40006400	N/A	N/A
I^2C2		0x40005800	APB1	0x40005800
I^2C1		0x40005400		0x40005400
UART5		0x40005000	N/A	N/A
UART4		0x40004C00	N/A	N/A
USART3		0x40004800	N/A	N/A
USART2		0x40004400		0x40004400
SPI2		0x40003800		0x40003800
WDT	APB1	0x40003000		0x40003000
WWDT		0x40002C00	APB1	0x40002C00
RTC		0x40002800		0x40002800
CMP		0x40002400		SCFG+0x1C
TMR14		0x40002000		0x40002000
TMR5		0x40000C00	N/A	N/A
TMR4		0x40000800	N/A	N/A
TMR3		0x40000400	APB1	0x40000400
TMR2		0x40000000	N/A	N/A

4.2 Functional differences

This section describes the peripheral differences in the AT32F421 series versus AT32F415 series. The peripheral behavior of the AT32F421 series is detailed in the subsections below.

4.2.1 FLASH interface

- *Table 5* presents the differences between AT32F421 series and AT32F415 in terms of Boot memory and User system data area.

Table 5. Flash memory address differences

Memory	AT32F415	AT32F421
Boot memory	0x1FFFAC00-0x1FFFF3FF	0x1FFFE400-0x1FFFF3FF
User system data area	0x1FFFF800-0x1FFFFBFF	0x1FFFF800-0x1FFFF9FF

As the control bit function of the FLASH_PSR register is different, the user just needs follow BSP library functions to operate while transiting from AT32F415 to AT32F421, without the need of manual change.

4.2.2 Interrupt vectors

- *Table 6* presents the interrupt vector differences in AT32F421 series versus AT32F415 series.

Table 6. Interrupt vector differences

Position	AT32F415	AT32F421
0	WDT	WDT
1	PVM	PVM
2	TAMPER	ERTC
3	ERTC	FLASH
4	FLASH	CRM
5	CRM	EXINT0_1
6	EXINT0	EXINT2_3
7	EXINT1	EXINT4_15
8	EXINT2	Reserved
9	EXINT3	DMA_CH1
10	EXINT4	DMA_CH2_CH3
11	DMA_CH1	DMA_CH4_CH5
12	DMA_CH2	ADC_CMP

Position	AT32F415	AT32F421
13	DMA_CH3	TMR1_BRK TMR1_UP TMR1_TRG TMR1_COM
14	DMA_CH4	TMR1_CH
15	DMA_CH5	Reserved
16	DMA_CH6	TMR3
17	DMA_CH7	TMR6
18	ADC1	Reserved
19	CAN1_TX	TMR14
20	CAN1_R0	TMR15
21	CAN1_R1	TMR16
22	CAN_SE	TMR17
23	EXINT5_9	I2C1_EVT
24	TMR1_BRK_TMR9	I2C2_EVT
25	TMR1_OVF_TMR10	SPI1
26	TMR1_TRG_HALL_TMR11	SPI2
27	TMR1_CH	USART1
28	TMR2	USART2
29	TMR3	Reserved
30	TMR4	Reserved
31	I2C1_EVT	Reserved
32	I2C1_ERR	I2C1_ERR
33	I2C2_EVT	Reserved
34	I2C2_ERR	I2C2_ERR
35	SPI1	Reserved

Position	AT32F415	AT32F421
36	SPI2	Reserved
37	USART1	Reserved
38	USART2	Reserved
39	USART3	Reserved
40	EXINT10_15	Reserved
41	ERTCAlarm	Reserved
42	OTGFS1	Reserved
43	Reserved	Reserved
44	Reserved	Reserved
45	Reserved	Reserved
46	Reserved	Reserved
47	Reserved	Reserved
48	Reserved	Reserved
49	SDIO	Reserved
50	TMR5	Reserved
51	Reserved	Reserved
52	UART4	Reserved
53	UART5	Reserved
54	Reserved	Reserved
55	Reserved	Reserved
56	DMA2_CH1	Reserved
57	DMA2_CH2	Reserved
58	DMA2_CH3	Reserved
59	DMA2_CH4_5	Reserved
60	Reserved	Reserved

Position	AT32F415	AT32F421
61	Reserved	Reserved
62	Reserved	Reserved
63	Reserved	Reserved
64	Reserved	Reserved
65	Reserved	Reserved
66	Reserved	Reserved
67	OTGFS	Reserved
68	Reserved	Reserved
69	Reserved	Reserved
70	CMP1	Reserved
71	CMP2	Reserved
72	ACC	Reserved

4.2.3 DMA interface

- *Table 7* presents the differences related to DMA in the AT32F421 series versus AT32F415 series.

Table 7. DMA interface differences

Peripheral	DMA request	AT32F415	AT32F421
TMR17	TMR17_UP TMR17_CH1	N/A	DMA_Channel1/DMA_Channel2 DMA_Channel1/DMA_Channel2
TMR16	TMR16_UP TMR16_CH1	N/A	DMA_Channel3/DMA_Channel4 DMA_Channel3/DMA_Channel4
TMR15	TMR15_UP TMR15_CH1 TMR15_TRIG TMR15_COM	N/A	DMA_Channel5 DMA_Channel5 DMA_Channel5 DMA_Channel5
USART1	USART1_Rx USART1_Tx	DMA1_Channel5 DMA1_Channel4	DMA_Channel3/DMA_Channel5 DMA_Channel2/DMA_Channel4
SPI1/I^2S1	SPI1/I2S1_Rx SPI1/I2S1_Tx	DMA1_Channel2 DMA1_Channel3	DMA_Channel2 DMA_Channel3

Peripheral	DMA request	AT32F415	AT32F421
TMR1	TMR1_UP TMR1_CH1 TMR1_CH2 TMR1_CH3 TMR1_CH4 TMR1_TRIG TMR1_COM	DMA1_Channel5 DMA1_Channel2 DMA1_Channel3 DMA1_Channel6 DMA1_Channel4 DMA1_Channel4 DMA1_Channel4	DMA_Channel5 DMA_Channel2 DMA_Channel3 DMA_Channel5 DMA_Channel4 DMA_Channel4 DMA_Channel4
ADC	ADC	DMA1_Channel1	DMA_Channel1 DMA_Channel2
I^2C2	I2C2_Rx I2C2_Tx	DMA1_Channel5 DMA1_Channel4	DMA_Channel5 DMA_Channel4
I^2C1	I2C1_Rx I2C1_Tx	DMA1_Channel7 DMA1_Channel6	DMA_Channel3 DMA_Channel2
SDIO	SDIO	DMA2_Channel4	N/A
USART2	USART2_Rx USART2_Tx	DMA1_Channel6 DMA1_Channel7	DMA_Channel5 DMA_Channel4
SPI2/I^2S2	SPI2/I2S2_Rx SPI2/I2S2_Tx	DMA1_Channel4 DMA1_Channel5	DMA_Channel4 DMA_Channel5
TMR6	TIM6_UP	N/A	DMA_Channel3
TMR3	TMR3_UP TMR3_CH1 TMR3_TRIG TMR3_CH3 TMR3_CH4	DMA1_Channel3 DMA1_Channel6 DMA1_Channel6 DMA1_Channel2 DMA1_Channel3	DMA_Channel3 DMA_Channel4 DMA_Channel4 DMA_Channel2 DMA_Channel3
TMR2	TMR2_UP TMR2_CH1 TMR2_CH2 TMR2_CH3 TMR2_CH4	DMA1_Channel2 DMA1_Channel5 DMA1_Channel7 DMA1_Channel1 DMA1_Channel7	N/A
TMR4	TMR4_UP TMR4_CH1 TMR4_CH2 TMR4_CH3	DMA1_Channel7 DMA1_Channel1 DMA1_Channel4 DMA1_Channel5	N/A

Peripheral	DMA request	AT32F415	AT32F421
UART4	UART4_Rx UART4_Tx	DMA2_Channel3 DMA2_Channel5	N/A
USART3	USART3_Rx USART3_Tx	DMA1_Channel3 DMA1_Channel2	N/A
TMR5	TMR5_UP TMR5_CH1 TMR5_CH2 TMR5_CH3 TMR5_CH4 TMR5_TRIG	DMA2_Channel2 DMA2_Channel5 DMA2_Channel4 DMA2_Channel2 DMA2_Channel1 DMA2_Channel1	N/A

- The AT32F415 series features flexible DMA mapping mode. In this mode, the DMA request can be remapped to any one of the 14 channels of DMA1 and DMA2. This feature is not available on AT32F421 series.

4.2.4 PWC interface

Table 8. PWC interface differences

PWC	AT32F415	AT32F421
Operating voltage	2.6~3.6V	2.4~3.6V
Power consumption at Deepsleep mode	In Deepsleep mode, the internal voltage regulator can be set in low-power mode to reduce power consumption	In Deepsleep mode, when the internal voltage regulator is set in low-power mode, it is also possible to enable extra low-power mode to further reduce power consumption
Wake-up pin from Standby mode	One WKUP pin	Four WKUP pins

- *Table 8* presents the difference between the PWR interface of the AT32F421 series and AT32F415 series. The AT32F421 series has made some optimizations in terms of power consumption so as to provide a wider range of power supply and further reduce the power consumption through additional bits. In addition, the AT32F421 series adds three WKUP pins (WKUP2-PC13, WKUP6-PB5 and WKUP7-PB15) to wake up from Standby modes in order to adapt to more application scenarios.

4.2.5 ADC interface

- *Table 9* presents the differences between the ADC interface of AT32F421 and AT32F415 series:

Table 9. ADC interface differences

ADC	AT32F415	AT32F421
Number of channels	16 channels + 2 internal channels	15 channels + 3 internal channels

Conversion mode	Repetition/Split/Sequence/Preempted modes		Repetition/Split/Sequence/Preempted modes	
Resolution	12-bit		12-bit	
External trigger	Regular group TMR1 CH1 TMR1 CH2 TMR1 CH3 TMR2 CH2 TMR3 TRGOUT TMR4 CH4 EXINT line11 OCSWTRG TMR1_TRGOUT	Preempted group TMR1 TRGOUT TMR1 CH1 TMR1 CH4 TMR2 CH1 TMR2 TRGOUT TMR3 CH4 TMR4 TRGOUT EXINT line15 PCSWTRG	Regular group TMR1 CH1 TMR1 CH2 TMR1 CH3 TMR3 TRGOUT TMR15 CH1 EXINT line11 OCSWTRG	Preempted group TMR1 TRGOUT TMR1 CH4 TMR3 CH4 TMR15 TRGOUT EXINT line15 PCSWTRG
Supply requirements	2.6 V to 3.6 V		2.4 V to 3.6 V	

4.2.6 EXINT interrupt source selection

- There are some differences between the external interrupt configuration mode of the AT32F415 series and AT32F421 series. The AT32F415 series uses the IOMUX_EXINTCx register to configure external interrupts, while AT32F421 series uses the SYSCFG_EXTICRx register. In this way, only the mapping address of the EXTICRx register has changed, without any change to the meaning of EXTIx configuration.

4.2.7 GPIO interface

- The differences related to GPIO alternate functions in the AT32F421 series versus AT32F415 series are described as follows:

  AT32F415:

  I/O alternate function configuration depends on the peripheral mode used. For instance, the USART Tx pin should be configured as alternate function push-pull, and the USART Rx should be input floating or input pull-up.

  To optimize the number of peripheral I/O functions on different packages, it is possible to remap some alternate functions to other pins. The IOMUX_REMAPx register is used to configure the alternate functions of the peripheral pins.

  AT32F421:

  It is required that the I/O pin is configured as alternate function for peripherals to use I/O functions properly.

  Pin multiplexing and mapping are configured through the GPIOx_MUXL and GPIOx_MUXH registers.

4.2.8 CMP interface

- ATT32F421 is not compatible with GX32E230 with respect to CMP control register. AT32F421 supports blanking output feature.

4.2.9 ERTC interface

- *Table 10* presents the ERTC differences between AT32F415 and AT32F421 series.

Table 10. ERTC interface differences

ERTC	AT32F415	AT32F421
Alarm clock B	Yes	No
Wake-up timer	Yes	No
Coarse digital calibration	Yes	No
Time stamp/tamper event EXTI line	EXINT 21	EXINT 19
Alarm interrupt channel	ERTC_Alarm IRQ	ERTC_IRQ
Time stamp/tamper event interrupt channel	TAMPER IRQ	

4.2.10 USART interface

- The AT32F421 series retains all the USART functions of the AT32F415 series, and adds the TX/RX SWAP feature (enabled by the register control bit SWAP). The SWAP allows to switch TX and RX pins, which is suitable for USART modes such as asynchronization, synchronization, single-wire half-duplex, smart card and IrDA.

4.2.11 Security library interface

- The security library of the AT32F421 is optimized compared to AT32F415 series. The AT32F21 series security library is divided into read-only area and instruction area without any address restriction.

4.2.12 Additional WKUP pins

- On top of the WKUP pin (WKUP1-PA0 pin of AT32F415), the AT32F421 also adds three WKUP pins dedicated to waking up from Standby mode. These four WKUP pins have their respective enable bits. When enabled, the wake-up event on the corresponding pin can wake up from Standby mode. It is possible to enable one or more wake-ups pins to wake up from Standby mode according to the actual application requirements.

4.2.13 Additional low-power consumption in Deepsleep mode

- In addition to the original internal voltage regulator switch (of AT32F415), the AT32F421 series also adds an extra low-power mode. This mode can further reduce power consumption of Deepsleep mode by lowering the output voltage of the voltage regular in the scenario when the internal voltage regulator is in low-power mode in Deepsleep mode.

4.2.14 Additional TMR15, TMR16 and TMR17 timers

- AT32F421 series adds TMR15, TMR16 and TMR17 timers.

4.2.15 Additional infrared transmitter

- This infrared transmitter is based on the internal connection between TMR16 and USART1, or USART2 and TMR17. The TMR17 is used to provide carrier frequency, while the TMR16, USART1 or USART2 provides the main signals to be sent. The infrared output signal is available on PB9 or PA13.

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
2022.02.28	2.0.0	Initial release
2022.05.30	2.0.1	Removed the repeated contents in Section 2.