MG0015
Migration Guide

Migrating from GX32E230 to AT32F421

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing GX32E230 series to AT32F421 series. It brings together the most important information and lists the vital aspects that need to be taken into account.

To move an application from GX32E230 series to AT32F421 series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F421xx

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1 Similarities and differences between AT32F421 and GX32E230

AT32F421 series microcontrollers are basically compatible with the GX32E230 series, and provide many enhanced features, some of which are different from GX32E230. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, define the alternate functions of the pins.
- Compiler tools: identical, for example, Keil, IAR.

1.2 Overview of differences

Table 1. Differences between AT32F421 and GX32E230

	AT32F421	GX32E230
Core	Cortex-M4 (without FPU)	Cortex-M23
Voltage range	2.4 V~3.6 V	1.8 V~3.6 V
System clock	Max frequency 120 MHz, APB1 120 MHz, APB2 120 MHz	Max frequency 72 MHz, APB1 72 MHz, APB2 72 MHz
Boot Memory	4 KB, support Flash memory content CRC	3 KB
Flash memory 16-bit write time	37 us	37 us
Flash memory page erase time	6.4 ms	1.1 ms
Flash memory mass erase time	8 ms	4 ms
SRAM size	8/16 KB by part number	4/6/8 KB by part number
SRAM parity check	NA	Support
GPIO locking	All GPIOs can be locked.	Only PA and PB can be locked.
PLL	Frequency multiplication factors from 31x to 500x; Frequency division factor from division by 1 to division by 15	Integer multiplication
I2S	2	1
4-wire SPI master mode	NA	1
ADC	2 Msps (max ADCCLK = 28 MHz)	2 Msps (max ADCCLK = 28 MHz)
USART wakeup	Not support	Wake up from deep sleep
Wake up from low-power mode (Voltage regular is in low-power mode)	450 us	17.1 us
Wake up from Standby mode	1250 us	77.5 us
Run mode	10.5 mA@72 MHz	8.5 mA@72 MHz
Power consumption at Sleep mode	7.76 mA@72 MHz	7.4 mA@72 MHz

	AT32F421	GX32E230
Power consumption at Deepsleep mode	210 uA	25.5 uA
Power consumption at Standby mode	3.6 uA	3.8 uA
Temperature range	-40 to +105 °C	-40 to +85 °C
Packages	Not support LGA20	Support LGA20

2 Hardware migration

The migration from AT32F421 to GX32E230 series is simple as they are pin-to-pin compatible for the same packages.

3 Software migration

3.1 Peripheral comparison

There are some differences between AT32F421 and GX32E230 in terms of peripherals, some of which are new designs for AT32F421 series. Therefore, it is necessary to modify these peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 2. Peripheral compatibility analysis

Peripheral	AT32F421	GX32E230	Compatibility	
			Pinout	Firmware driver
SPI	Y	Y	Partially same	Partial compatibility
WWDT	Y	Y	NA	Full compatibility
WDT	Y	Y	NA	Partial compatibility
DEBUG	Y	Y	NA	Partial compatibility
CRC	Y	Y	NA	Partial compatibility
EXINT	Y	Y	Identical	Partial compatibility
DMA	Y	Y	NA	Partial compatibility
TMR	Y	Y	Identical	Partial compatibility
PWC	Y	Y	NA	Partial compatibility
USART	Y	Y	Identical	Incompatible
I2C	Y	Y	Identical	Partial compatibility
ADC	Y	Y	Identical	Partial compatibility
RTC	Y	Y	Identical	Partial compatibility
FLASH	Y	Y	NA	Partial compatibility
GPIO	Y	Y	Identical	Partial compatibility
CMP	Y	Y	Partially same	Incompatible
SCFG	Y	Y	Identical	Partial compatibility

3.2 Memory mapping

AT32F421 architecture is highly compatible with GX32E230, except the distribution of peripheral addresses and buses as shown in *Table 3*.

Table 3. Memory map differences

Peripheral	GX32E230		AT32F421	
	Bus	Base address	Bus	Base address
DEBUG	APB2	0x40015800	CPU core	0xE0042000

3.3 Functional differences

This section describes the peripheral differences between AT32F421 and GX32E230.

3.3.1 CRM interface

- The differences related to CRM (Clock and reset management) in the AT32F421 series versus GX32E230 are presented in *Table 4*.

Table 4. CRM differences

CRM	GX32E230	AT32F421
HICK	8 MHz RC	48 MHz RC divided by 6
HEXT	4-32 MHz	4-25 MHz
HICK14	28 MHz RC for ADC	NA
HICK48	NA	48 MHz RC
CLKOUT	HICK28, LICK, LEXT, HICK, HEXT, PLL and PLL/2	ADCCLK, SYSCLK, LICK, LEXT, HICK, HEXT, PLL/2 and PLL/4

3.3.2 DMA interface

- The differences related to DMA in AT32F421 series versus GX32E230 are presented in *Table 5*.

Table 5. DMA differences

Peripheral	DMA request	GX32E230	AT32F421
I2S2	I2S2_Rx	NA	DMA1_Channel2
	I2S2_Tx	NA	DMA1_Channel3
I2S2	I2S2_Rx	NA	DMA1_Channel2
	I2S2_Tx	NA	DMA1_Channel3

3.3.3 GPIO interface

- The main difference related to GPIO between AT32F421 and GX32E230 is that the AT32F421 output mode does not support internal pull-up and pull-down.

Table 6. GPIO differences

GPIO	GX32E230	AT32F421
Output mode	PP	PP
	PP+PU	
	PP+PD	
	OD	OD
	OD+PU	
	OD+PD	
Alternate function	PP	PP
	PP+PU	
	PP+PD	
	OD	OD
	OD+PU	
	OD+PD	

3.3.4 ADC interface

- *Table 7* presents the differences related to ADC between AT32F421 series and GX32E230 series:

Table 7. ADC differences

ADC	GX32E230	AT32F421
Number of channels	10 channels + 2 internal channels	15 channels + 3 internal channels
Resolution	6/8/10/12-bit	Fixed 12-bit
Clock	Dual clock domain (APB clock and HSI28 clock)	APB clock
Oversampling	Hardware oversampling	Software oversampling

3.3.5 USART interface

- The USART peripheral in the AT32F421 is different from that of GX32E230 as they have different programming procedures, features and structure. Thus the code written for the GX32E230 series using the USART needs to be rewritten to run on AT32F421 series.

3.3.6 CRM PLL

- For AT32F421, it is necessary to configure the PLL_FREF parameters (CRM_PLL [26:24] bit) in the reference configuration table according to the PLL clock source used before programming and enabling CRM PLL.

3.3.7 FLASH interface

- The Flash memory differences between AT32F421 and GX32E230 are shown in *Table 8* .

Table 8. Flash memory differences

SYSCLK Range	GX32E230	AT32F421
Zero wait	0 MHz < SYSCLK <= 24 MHz	0 MHz < SYSCLK <= 32 MHz
One wait	24 MHz < SYSCLK <= 48 MHz	32 MHz < SYSCLK <= 64 MHz
Two waits	48 MHz < SYSCLK <= 72 MHz	64 MHz < SYSCLK <= 96 MHz
Three waits	NA	96 MHz < SYSCLK <= 120 MHz

3.3.8 SPI interface

- AT32F421 removes the following SPI features versus GX32E230:

1. TI mode configuration
2. NSSP mode configuration
3. TxRx buffers
4. SPI1 master mode extended QSPI
5. Configurable Frame Size

AT32F421 has additional features as follows:

1. SPI can be used as I2S feature
2. Support real-time synchronization between I2S WS and Data
3. SPI speed up to 50 MHz

3.3.9 CMP interface

- AT32F421 is not compatible with GX32E230 with respect to CMP control register. AT32F421 supports blanking output feature.

3.3.10 RTC interface

- AT32F421 only supports tamper detection 0 (tamper0), not tamper 1, compared to GX32E230.

3.3.11 Security library (sLib)

- Security library (sLib) feature is provided to prevent important IP-code from being modified or read by end applications so as to enhance security level.

3.3.12 GPIO 5V-tolerant compatibility

- AT32F421 provides more 5V-tolerant input pins compared to GX32E230, except PC14, PC15, PF0 and PF1 (the input level of these pins should not exceed VDD + 0.3V).
- All other pins are 5V-tolerant.

4 Revision history

Table 9. Document revision history

Date	Revision	Changes
2022.02.25	2.0.0	Initial release

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