MG0014
Migration Guide

Migrating from GX32F330 to AT32F421

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing GX32F330 series to AT32F421 series device. It puts together the most important information and lists the vital aspects that need to be taken into account.

To move an application from GX32F330 series to AT32F421 series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F421xx

Contents

1 Similarities and differences between AT32F421 and GX32F330 4

1.1 Overview of similarities 4

1.2 Overview of differences 4

2 Hardware migration 6

3 Software migration 7

3.1 Peripheral comparison 7

3.2 Memory mapping 7

3.3 Functional differences 7

3.3.1 CRM 8

3.3.2 DMA interface 8

3.3.3 Interrupt vectors 8

3.3.4 GPIO interface 9

3.3.5 ADC interface 9

3.3.6 USART interface 9

3.3.7 CRM PLL 9

3.3.8 FLASH interface 10

3.3.9 SPI interface 10

3.3.10 RTC interface 10

3.3.11 PWC 10

3.3.12 Security library (sLib) 10

3.3.13 GPIO 5V-tolerant compatibility 10

4 Revision history 11

List of tables

Table 1. Differences between AT32F421 and GX32F330 4
Table 2. Pin compatibility between AT32F421 and GX32F330 6
Table 3. Peripheral compatibility analysis 7
Table 4. Memory map differences 7
Table 5. CRM differences 8
Table 6. DMA differences 8
Table 7. Interrupt vector differences 8
Table 8. GPIO differences 9
Table 9. ADC differences 9
Table 10. Flash Flash memory differences 10
Table 11. Document revision history 11

1 Similarities and differences between AT32F421 and GX32F330

AT32F421 series microcontrollers are basically compatible with the GX32F330 series, and provide many enhanced features, some of which are different from GX32F330. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, the alternate function of pins are defined
- Compiler tools: identical, for example, Keil, IAR

1.2 Overview of differences

Table 1. Differences between AT32F421 and GX32F330

	AT32F421	GX32F330
Core	Cortex-M4 (without FPU)	Cortex-M4 (with FPU)
Voltage range	2.4 V~3.6 V	2.6 V~3.6 V
VBAT supply	Not support	Support
System clock	Max frequency 120 MHz, APB1 120 MHz, APB2 120 MHz	Max frequency 84 MHz, APB1 42 MHz, APB2 42 MHz
Boot Memory	4 KB, support Flash memory content CRC check	3 KB
Flash memory 16-bit write time	37 us	>200 us
Flash memory sector erase time	6.4 ms	100 ms
Flash memory mass erase time	8 ms	>3.2 s
SRAM size	8/16 KB by part number	4/8 KB by part number
SRAM parity check	NA	Support
GPIO locking	All GPIOs can be locked.	Only PA and PB can be locked.
PLL	Frequency multiplication factors from 31x to 500x; Frequency division factor from division by 1 to division by 15	Integer multiplication
I2S	2	1
4-wire SPI master mode	NA	1
32-bit timer	NA	TMR2
ADC	2 Msps (max ADCCLK = 28 MHz)	2.86 Msps (max ADCCLK = 40 MHz)
Basic timer	TMR6	NA
USART wakeup	Not support	Wake up from deep sleep mode
Run mode	15.2 mA@108 MHz	19.86 mA@84 MHz
Power consumption at Sleep mode	11.1 mA@108 MHz	10.60 mA@84 MHz

	AT32F421	GX32F330
Power consumption at Deepsleep mode	210 uA	92 uA
Power consumption at Standby mode	3.6 uA	6.85 uA
Temperature range	-40 to +105 °C	-40 to +85 °C
Packages	Up to LQFP48	Up to LQFP64

2 Hardware migration

The migration from AT32F421 to GX32F330 series is simple as because they are pin-to-pin compatible basically, with only a few pins being affected.

Table 2. Pin compatibility between AT32F421 and GX32F330

AT32F421					GX32F330				
TSSOP20	QFN28	QFN32	LQFP48	Pin name	TSSOP20	QFN28	QFN32	LQFP48	Pin name
-	-	-	1	VDD	-	-	-	1	VBAT

3 Software migration

3.1 Peripheral comparison

In terms of peripherals, there are some differences between AT32F421 and GX32F330, and some of them are new designs for AT32F421. Therefore, it is necessary to modify peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 3. Peripheral compatibility analysis

Peripheral	AT32F421	GX32F330	Compatibility	
			Pinout	Firmware driver
SPI	Y	Y	Identical	Partial compatibility
WWDT	Y	Y	NA	Full compatibility
WDT	Y	Y	NA	Partial compatibility
DEBUG	Y	Y	NA	Partial compatibility
CRC	Y	Y	NA	Partial compatibility
EXINT	Y	Y	Identical	Partial compatibility
DMA	Y	Y	NA	Partial compatibility
TMR	Y	Y	Identical	Partial compatibility
PWC	Y	Y	NA	Partial compatibility
USART	Y	Y	Identical	Incompatible
I2C	Y	Y	Identical	Partial compatibility
ADC	Y	Y	Identical	Partial compatibility
RTC	Y	Y	Identical	Partial compatibility
FLASH	Y	Y	NA	Partial compatibility
GPIO	Y	Y	Identical	Partial compatibility
CMP	NA	Y	NA	NA
SCFG	Y	Y	Identical	Partial compatibility

3.2 Memory mapping

AT32F421 architecture is highly compatible with GX32F330, except the distribution of peripheral addresses and buses as shown in *Table 4*.

Table 4. Memory map differences

Peripheral	GX32F330		AT32F421	
	Bus	Base address	Bus	Base address
GPIOD	AHB2	0x48000C00	NA	NA
CTC	APB1	0x4000C800	NA	NA
TMR6	NA	NA	APB1	0x40001000
TMR2	APB1	0x40000000	NA	NA

3.3 Functional differences

This section describes the peripheral differences between AT32F421 and GX32F330.

3.3.1 CRM

- The differences related to CRM (Clock and reset management) in the AT32F421 series versus GX32F330 are presented in *Table 5*.

Table 5. CRM differences

CRM	GX32F330	AT32F421
HICK	8 MHz RC	48 MHz RC divided by 6
HEXT	4-32 MHz	4-25 MHz
HICK14	28 MHz RC ADC	NA
HICK48	NA	48 MHz RC
CLKOUT	HICK28, LICK, LEXT, HICK, HEXT, PLL, PLL/2	ADCCLK, SYSCLK, LICK, LEXT, HICK、HEXT, PLL/2, PLL/4

3.3.2 DMA interface

- The differences related to DMA in AT32F421 series versus GX32F330 are presented in *Table 6*.

Table 6. DMA differences

Peripheral	DMA request	GX32F330	AT32F421
TMR2	TMR2_UP TMR2_CH1 TMR2_CH2 TMR2_CH3 TMR2_CH4	DMA_Channel2 DMA_Channel5 DMA_Channel3 DMA_Channel1 DMA_Channel4	NA
TMR6	TMR6_UP	NA	DMA_Channel3

3.3.3 Interrupt vectors

- *Table 7* presents the interrupt vectors and interrupt vector number in AT32F421 series versus GX32F330.

Table 7. Interrupt vector differences

Position	GX32F330	AT32F421
15	TMR2	Reserved
17	Reserved	TMR6
48	DMA_CH6_CH7	Reserved

3.3.4 GPIO interface

- The main difference related to GPIO between AT32F421 and GX32F330 is that the AT32F421 output mode does not support internal pull-up and pull-down.

Table 8. GPIO differences

GPIO	GX32F330	AT32F421
Output mode	PP PP+PU PP+PD OD OD+PU OD+PD	PP OD
Alternate function	PP PP+PU PP+PD OD OD+PU OD+PD	PP OD

3.3.5 ADC interface

- *Table 9* presents the differences related to ADC interface between AT32F421 series and GX32F330 series:

Table 9. ADC differences

ADC	GX32F330		AT32F421	
Number of channels	16 channels +3 internal channels		15 channels +3 internal channels (without V_{BAT} channel but with V_{SSA} channel)	
Clock	Dual clock domain (APB clock and HICK14 clock)		APB clock	
External Trigger	Regular group TMR2 CC2	Preempted group TMR2 TRGO TMR2 CC1	Regular group NA	Preempted group NA NA
Supply requirement	2.6 V to 3.6 V		2.4 V to 3.6 V	

3.3.6 USART interface

- The USART peripheral of the AT32F421 has big difference versus GX32F330. The AT32F421 programming procedures, features and structure are different from those of the GX32F330, so the code written for the GX32F330 series using the USART needs to be rewritten to run on AT32F421 series.

3.3.7 CRM PLL

- For AT32F421, it is necessary to configure the PLL_FREF parameters (CRM_PLL[26:24]) in the reference configuration table according to the PLL clock source used before programming and enabling CRM PLL.

3.3.8 FLASH interface

- The Flash memory differences between AT32F421 and GX32F330 are shown in *Table 10*.

Table 10. Flash Flash memory differences

SYSCLK Range	GX32F330	AT32F421
0 MHz < SYSCLK <= 32 MHz	NA	Zero wait
32 MHz < SYSCLK <= 64 MHz		One wait
64 MHz < SYSCLK <= 96 MHz		Two waits
96 MHz < SYSCLK <= 120 MHz		Three waits

3.3.9 SPI interface

- AT32F421 removes the following SPI features versus GX32F330:

1. TI mode configuration
2. NSSP mode configuration
3. SPI1 master mode extended QSPI

AT32F421 has additional features as follows:

1. SPI can be used as I2S
2. Supports synchronization between I2S WS and Data
3. SPI speed up to 50 MHz

3.3.10 RTC interface

- AT32F421 only supports tamper detection 0 (tamper0), not tamper 1, compared to GX32F330.

3.3.11 PWC

- Unlike GX32F330, AT32F421 cancels PC5 as a wkup pin
- Unlike GX32F330, AT32F421 removes high/low driving mode switch feature

3.3.12 Security library (sLib)

- Security library (sLib) feature is provided to prevent important IP-code from being modified or read by end applications so as to enhance security level.

3.3.13 GPIO 5V-tolerant compatibility

- AT32F421 provides more 5V-tolerant input pins, except PC14, PC15, PF0 and PF1 (the input level of these pins should not exceed VDD + 0.3V).
- All other pins are 5V-tolerant.

4 Revision history

Table 11. Document revision history

Date	Revision	Changes
2022.02.25	2.0.0	Initial release
2022.10.17	2.0.1	Added *3.3.11 PWC*

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Purchasers are solely responsible for the selection and use of ARTERY's products and services, and ARTERY assumes no liability whatsoever relating to the choice, selection or use of the ARTERY products and services described herein.

No license, express or implied, to any intellectual property rights is granted under this document. If any part of this document deals with any third party products or services, it shall not be deemed a license grant by ARTERY for the use of such third party products or services, or any intellectual property contained therein, or considered as a warranty regarding the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

Unless otherwise specified in ARTERY's terms and conditions of sale, ARTERY provides no warranties, express or implied, regarding the use and/or sale of ARTERY products, including but not limited to any implied warranties of merchantability, fitness for a particular purpose (and their equivalents under the laws of any jurisdiction), or infringement of any patent, copyright or other intellectual property right.

Purchasers hereby agrees that ARTERY's products are not designed or authorized for use in: (A) any application with special requirements of safety such as life support and active implantable device, or system with functional safety requirements; (B) any air craft application; (C) any automotive application or environment; (D) any space application or environment, and/or (E) any weapon application. Purchasers' unauthorized use of them in the aforementioned applications, even if with a written notice, is solely at purchasers' risk, and is solely responsible for meeting all legal and regulatory requirement in such use.

Resale of ARTERY products with provisions different from the statements and/or technical features stated in this document shall immediately void any warranty grant by ARTERY for ARTERY products or services described herein and shall not create or expand in any manner whatsoever, any liability of ARTERY