MG0007
Migration Guide

Migrating from SXX32F103 to AT32F403A

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing SXX32F103 series to AT32F403A series device. It puts together the most important information and lists the vital aspects that need to be taken into account.

To move an application from SXX32F103 series to AT32F403A series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F403Axx

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1 Similarities and differences between AT32F403A and SXX32F103

The AT32F403A series microcontrollers are basically compatible with the SXX32F103 series and provide many enhanced features, some of which are slightly different from the SXX32F103 series. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: The same package has the same pin definition. For extended peripherals, the alternate function of pins are defined.
- Addressing space: Memory and registers have the same logical addresses. Extended peripherals occupy the reserved space of SXX32 series.
- Compiler tools: identical, for example, Keil, IAR

1.2 Overview of differences

Table 1. Differences between AT32F403A and SXX32F103

	AT32F403A	SXX32F103xC/xB/x8
Core	Cortex-M4, DSP instruction and Floating Point Unit (FPU)	Cortex-M3
System clock	Max frequency 240 MHz, both APB1 and APB2 are 120 MHz	Max frequency 72 MHz, APB1 36 MHz, APB2 72 MHz
Startup	13 ms	2.5 ms
Reset	8 ms	-
Wake up from Standby mode	8 ms	50 us
SRAM size	Up to 224 KB	96 KB
External SPI Flash	External SPI flash (SPIM), up to 16M Bytes	Not support
Boot Memory	18 KB boot memory has more features than SXX32F103: 1. USB DFU ISP programming 2. SPIM ISP programming 3. Flash memory CRC check	6KB/2KB by part number
User System Data	48 Bytes user system data with the below features: 1. SRAM mode settings 2. 8 Bytes SPIM encryption key 3. Custom field (such as developer ID)	16 Bytes
Flash memory 16-bit write time	50 µs	52.5 µs
Flash memory page erase time	50 ms	40 ms
Flash memory mass erase time	0.8 s (AT32F403AxC) 1.4 s (AT32F403AxE) 2.8 s (AT32F403AxG)	40 ms

	AT32F403A	SXX32F103xC/xB/x8
Security library (sLib)	Support	NA
Battery powered register	42 x half-word battery powered registers	10 x for medium and low density
Extended I2C	Support I2C	I2C1/2
Extended SPI	Support SPI4	SPI1/2/3
Extended SDIO	Support SDIO2	SDIO1
Extended USART and UART	Support USART6/UART7/UART8	Not support USART6/UART7/UART8
SPI1 used as I2S	SPI1 can be used as I2S	SPI1 can be used as SPI only
I2S support	48-pin package has I2S I2S2/3 full-duplex support	48-pin has no I2S Not support I2S full-duplex
Extended CAN2	Support CAN2	Not support CAN2
Simultaneous use of CAN and USB	Support	Not support
Extended 48 MHz HICK supports USB peripheral	Support	Not support
HICK auto clock calibration (ACC)	Support	Not support
XMC	1. Support NOR/PSRAM of the alternate signals or support NOR/PSRAM of the non-alternate signals via external device (Refer to AN0068) 2. 2 chip select 3. Not support external interrupts 64-pin package supports 8-bit LCD parallel interface	1. Support CF card and NOR/SRAM/PSRAM 2. 4 chip select 3. Support 2 external interrupts 64-pin packages do not support.
Flash memory CRC check	Support	Not support
High-speed GPIO	GPIO is on AHB bus	GPIO is on APB bus
Extended memory interface	64-pin and more packages support bus output (XMC)	Only 144-pin package, and 256 KB and more support bus output
32-bit timer	TMR2 and TMR5 are 32-bit timers	All 16 bits
USB buffer	Up to 768 Byte	512 Byte
ADC	2 Msps (max ADCCLK = 28 MHz)	1 Msps (max ADCCLK = 14 MHz)
ADC trigger event	Support TMR1, TMR8 and TMR15	No TMR15
Temperature sensor	Positive temperature factor	Negative temperature factor
Voltage range	2.6V~3.6V	2.0V~3.6V
Ambient temperature TA	-40°C~+105°C	-40°C~+85°C
Core voltage	1.2V	1.8V
ESD parameters	HBM:5KV, CDM:1000V	HBM:2KV, CDM:500V
Run mode	37.1 mA @ 72MHz	51 mA @ 72MHz
Power consumption at	31.8 mA @ 72MHz	29.5mA @ 72MHz

	AT32F403A	SXX32F103xC/xB/x8
Sleep mode		
Power consumption at Deepsleep mode	1.4 mA	25 uA
Power consumption at Standby mode	5.7 uA	2.1 uA

2 Hardware migration

The migration from SXX32F103 to AT32F403A series is very simple as they are pin-to-pin compatible basically.

3 Software migration

3.1 Functional enhancement

This section describes the enhanced peripheral features of AT32F403A versus SXX32F103. The subsection presents the behavior of the AT32F403A.

3.1.1 ARM® 32-bit Cortex®-M4F with FPU

- Memory Protection Unit (MPU)
- Built-in single-cycle multiplication and hardware division
- Floating Point Unit (FPU)
- DSP instruction set

3.1.2 Security library

- Security library (sLib) feature is provided to prevent important IP-code from being modified or read by end applications so as to enhance security level.

3.1.3 High frequency PLL settings

- AT32F403A embeds a PLL that can output up to 240 MHz clock, with slight different in terms of settings
- PLL supports two frequency band, bordered by 72 MHz. Its frequency can be up to 240 MHz by setting the PLLRANG register according to the output frequency

3.1.4 Extended prescaler

- USB prescaler supports /2, /2.5, /3, /3.5, /4 output
- ADC prescaler supports /12, /16 output
- HEXT prescaler supports /3, /4, /5 output
- Main clock output (CLKOUT) supports CLKOUT precaler feature to obtain CLKOUT/2. CLKOUT/4…CLKOUT/512
- Main clock output (CLKOUT) supports LEXT, LICK, PLLCLK/4, USB48M, ADCCLK output

3.1.5 Internal memory size extension

- Internal memory can be extended from 96 KB to 224 KB. If this mode is enabled, the address space of the corresponding zero-wait Flash memory to be limited to 128 KB.

3.1.6 External SPI Flash (SPIM feature)

- Support external SPI Flash as Flash extension area.

3.1.7 SDIO2 support

- Add SDIO2 support

3.1.8 I2C3 support

- Add I2C3 support

3.1.9 SPI4 support

- Add SPI4/I2S4 support

3.1.10 I2S full-duplex support

- Add two modules (I2S2_ext and I2S3_ext) supporting I2S full-duplex mode

3.1.11 Extended USART and UART

- Support USART6/UART7/UART8

3.1.12 CAN2 support

- Add CAN2 support

3.1.13 Simultaneous use of CAN and USB

- CAN and USB can be used at the same time.
- CAN has its individual 512-byte SRAM memory
- USB also has its individual SRAM space, and the disabled CAN space can be assigned to USB

3.1.14 32-bit timer

- TMR2/TMR5 can be configured as 32-bit timers.

3.1.15 SPI1 used as I2S1

- SPI1 can be used as I2S1.

3.1.16 USBDEV buffer

- USB device (USBDEV) buffer can be extended to 768 / 1024 / 1280 Bytes.

3.1.17 48MHz HICK supports USB peripheral

- 48 MHz clock can be used for the USB peripheral.

3.1.18 HICK auto clock calibration (ACC)

- ACC module, auto clock calibration (HICK ACC) uses the SOF signal (1 ms cycle) generated from the USB module as a reference signal for the sampling and calibration of the HICK clock.

3.1.19 64-pin package supports XMC

- 64-pin packages support XMC, but XMC only supports 8-bit 8080/6800 mode to drive LCD

3.1.20 Flash memory CRC check

- Flash memory CRC check is supported.

3.1.21 High-speed GPIO

- GPIO is optimized to put the GPIO clocks on the AHB bus.

3.1.22 Additional DMA flexible mapping request feature

- DMA1/DMA2 comes with flexible mapping request feature.

3.1.23 CRC peripheral

- AT32 CRC peripheral allows to reverse the bit position of input data according to a given data format (byte, half-word or word). In other words, the upper bit of an input data is reversed to a lower bit, and so on.
- AT32 CRC peripheral supports reversing the bit location of an output data according to the full-word format. In other words, the upper bit of an output data is reversed to a lower bit, and so on.

3.2 Peripheral differences

This section describes the peripherals differences between AT32F403A and SXX32F103. The behavior of the AT32F403A is detailed in subsections.

3.2.1 High frequency PLL settings

- When the embedded PLL is greater than 108 MHz in AT32F403A, it is necessary to use auto step-by-step frequency switch feature.

3.2.2 Internal temperature sensor

- Temperature sensor has positive temperature factors.

3.2.3 GPIO 5V-tolerant pin compatibility

- PA11 and PA12 on all packages, and PD0 and PD1 on 64-pin/48-pin packages are not 5V tolerant, so the input level of these pins must not exceed VDD + 0.3V.

3.2.4 BOOT0 with a pull-down resistor

- BOOT0 embeds a pull-down resistor of around 90 KΩ (cannot be disabled), therefore it is not necessary to add an external pull-down resistor while using BOOT0 pin.

3.2.5 PA0 pull-down resistor auto enable in Standby mode

- When the Standby mode is being entered, the pull-down resistor of PA0 pin is automatically enabled by internal control circuitry of the chip. The reason of this is to avoid current leakage caused by pin floating.

3.2.6 USB_DP with internal pull-up resistor

- USB_DP has an internal pull-down resistor supporting full-speed device. Thanks to this, users do not need an external 1.5kΩ pull-up resistor.

3.2.7 Dual CAN filter banks

- CAN1 and CAN2 are mutually independent, each of which has a fixed set of 14 filter banks.

3.2.8 XMC usage differences

As the AT32F403A offers the largest 100-pin package, this cause some differences in XMC functions between AT32F403 and SXX32F103 in case of their respective largest package.

Table 2. XMC functional differences

MCU	Address/data lines alternate function	Bank support	Memory support
SXXF103	Non-multiplexed / multiplexed mode support	Bank: support bank1/2/3/4	SRAM/PSRAM/NOR FLASH/NAND FLASH/PC card
AT32F403A	Multiplexed mode only	Bank: support bank1/2	Multiplexed PSRAM/multiplexed NOR FLASH

4 Revision history

Table 3. Document revision history

Date	Revision	Changes
2022.02.25	2.0.0	Initial release
2022.10.19	2.0.1	1. Added *3.1.23 CRC peripheral* 2. Added *3.2.8 XMC usage differences*

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