USB 48 MHz clock failure when enable/disable PLL

Questions:

When PLL division is used to clock 48 MHz for USB, the USB divider error might occur (even if probability is very low) during enable/disable PLL, causing USB unable to work normally due to loss of 48 MHz clock.

Answer：

Solution 1:

There are two clock sources — PLL division or HICK 48 MHz, to provide 48 MHz to USB controller. Therefore users can choose HICK 48 MHz as a clock source of USB while enabling ACC for automatic clock calibration.

Here is the code for selecting HICK as USB clock source.

```
usb_clock48m_select(USB_CLK_HICK);
```

Solution 2:

If PLL division must be used to provide 48 MHz to USB, users can use the status of USB to judge whether the current clock is running normal or not.

After USB initialization, interrupts such as Suspend, Reset, SOF, Wakeup and TC (transfer complete) will be enabled by default. If no any interrupt other than wakeup (wakeup interrupt can still be generated without USB clock) is detected within 200ms, it indicates a USB clock exception, and needs to restore it through system reset.

Code modification are as follows:

- Add the following code to the usbd_irq_handler. It means that if no any interrupt (excluding wakeup interrupt) is detected, a flag "*usb_clock_flag=1*" is set, indicating USB OK.

```
if((sts_val & USB_WK_FLAG) == 0)
{
    usb_clock_flag = 1;
}
```

- Wait for 200ms after USB initialization, if the *usb_clock_flag* is not set (*usb_clock_flag* is not 1), it suggests USB clock error and needs a system reset.

```
usbd_connect(&usb_core_dev);

delay_ms(200);

if(usb_clock_flag == 0)
{
    nvic_system_reset();
}
```

Type: MCU application

Applicable products: AT32F413, AT32F403A, AT32F407, AT32A403A

Main function: USB

Other function: None

Document revision history

Date	Revision	Changes
2022.5.18	2.0.0	Initial release

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