ARM®-based 32-bit Cortex®-M4 MCU with FPU, 128 to 256 KB Flash, sLib, 14 timers, 1 ADC, 19 communication interfaces (CAN, OTGHS, OTGFS)

Features

- **Core: ARM® 32-bit Cortex®-M4 CPU with FPU**
  - 216 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication and hardware division
  - Floating point unit (FPU)
  - DSP instructions
- **Memories**
  - 128 to 256 KBytes of internal Flash memory
  - 20 Kbytes of boot memory used as a Bootloader or as a general instruction/data memory (one-time programmable)
  - sLib: configurable part of main Flash as a library area with code executable but secured, non-readable
  - 70 to 102 KBytes of SRAM (the first 48 KB with parity check)
  - QSPI interface for interfacing external SPI memory or SPI RAM extension, supporting address mapping mode
- **Power control (PWC)**
  - 2.4 to 3.6 V supply
  - Power on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep, and Standby modes
  - 20x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal (HEXT)
  - 48 MHz internal factory-trimmed high speed clock (HICK), ±1% accuracy at T_A = 25 °C and ±2.5% accuracy at T_A = -40 °C to +105 °C, with automatic clock calibration (ACC)
  - 32 kHz crystal (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 1x 12-bit 2 MSPS A/D converter, up to 16 external input channels; hardware over-sampling up to equivalent 16-bit resolution
  - Temperature sensor (V_{TS}), internal reference voltage (V_{INTRV})
- **DMA**
  - 2x 7-channel DMA controllers with flexible mapping capability
- **Up to 56 fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 14 timers (TMR)**
  - 1x 16-bit 7-channel advanced timer, including 3 pairs of complementary PWM outputs with dead-time generator and emergency break
  - Up to 7x 16-bit + 1x 32-bit general-purpose timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature encoder input
  - 2x 16-bit basic timers
  - 2x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with auto-wakeup, alarm, subsecond accuracy, and hardware calendar, calibration feature**
- **Up to 19 communication interfaces**
  - Up to 3x I^2C interfaces (SMBus/PMBus)
  - Up to 3x SPIs (36 Mbit/s), all with multiplexed half-duplex I^2S; 2x half-duplex I^2S combined for full-duplex mode
  - 1x independent full-duplex I^2S (I^2SF)
  - Up to 6x USARTs and 2x UARTs, support master synchronization SPI and modem control, ISO7816 interface, LIN, IrDA, and RS485 driver enable, TX/RX swap
  - 1x CAN (2.0B Active) with dedicated 256KB buffer
  - 1x OTGHS high speed controller with on-chip PHY, dedicated 4 KB buffer (for AT32F405 only)
  - 1x OTGFS full speed controller with on-chip PHY, dedicated 1280 KB buffer, supporting crystal-less in device mode
  - Infrared transmitter (IRTMR)
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Debug mode**
  - SWD and SWO interfaces
- **Operating temperatures: -40 to +105 °C**

- **Packages**
  - LQFP64 10 x 10 mm
  - LQFP64 7 x 7 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm
  - QFN32 4 x 4 mm

Table 1. AT32F405 device summary

Internal Flash	Part number
256 KBytes	AT32F405RCT7, AT32F405RCT7-7, AT32F405CCT7, AT32F405CCU7, AT32F405KCU7-4
128 KBytes	AT32F405RBT7, AT32F405RBT7-7, AT32F405CBT7, AT32F405CBU7, AT32F405KBU7-4

Table 2. AT32F402 device summary

Internal Flash	Part number
256 KBytes	AT32F402RCT7, AT32F402RCT7-7, AT32F402CCT7, AT32F402CCU7, AT32F402KCU7-4
128 KBytes	AT32F402RBT7, AT32F402RBT7-7, AT32F402CBT7, AT32F402CBU7, AT32F402KBU7-4

Contents

List of tables

List of figures

1 Descriptions

The AT32F405/402 series are based on the high-performance ARM®Cortex®-M4 32-bit RISC core operating at a frequency of up to 216 MHz. The Cortex®-M4 core features a single-precision Floating point unit (FPU) supporting all ARM® single-precision data processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) that enhances application security.

The AT32F405/402 series incorporate high-speed on-chip memories (up to 256 KBytes of internal Flash memory, 96+6 KBytes of SRAM), and a wide range of enhanced GPIO ports and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib” (security library), functioning as a security area with code-executable only. In addition, the AT32F405/402 devices include a high-level memory extension: quad SPI memory interface (QSPI).

The AT32F405/402 series offer one 12-bit ADC, seven general-purpose 16-bit timers plus one general-purpose 32-bit timer, two basic timers, one advanced timer and one low-power ERTC. They also feature standard and advanced communication interfaces: up to three I^2Cs, three SPIs (multiplexed as half-duplexed I^2Ss), one full-duplexed I^2SF interface, six USARTs, two UARTs, one CAN, and OTGHS interface (with on-chip PHY for AT32F405 only), one OTGFS interface, and one infrared transmitter.

The AT32F405/402 series operate in the -40 to +105 °C temperature range, from a 2.4 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

The AT32F405/402 devices are supplied in different package types. They are fully pin-to-pin, software and functionally compatible throughout the AT32F405/402 series, except that the configurations of peripherals are not fully identical depending on the package types.

Table 3. AT32F405 features and peripheral counts

Part number		AT32F405xxU7-4		AT32F405xxU7		AT32F405xxT7		AT32F405xxT7-7		AT32F405xxT7	
		KB	KC	CB	CC	CB	CC	RB	RC	RB	RC
Frequency (MHz)		216									
Internal Flash (KB)		128	256	128	256	128	256	128	256	128	256
SRAM (KB)		64+6	96+6	64+6	96+6	64+6	96+6	64+6	96+6	64+6	96+6
QSPI		1		1		1		1		1	
Timers	Advanced	1		1		1		1		1	
	32-bit general-purpose	1		1		1		1		1	
	16-bit general-purpose	7		7		7		7		7	
	Basic	2		2		2		2		2	
	SysTick	1		1		1		1		1	
	WDT	1		1		1		1		1	
	WWDT	1		1		1		1		1	
	ERTC	1		1		1		1		1	
Communication interfaces	I^2C	3		3		3		3		3	
	SPI(1)	2(3)		3		3		3		3	
	I^2S(half-duplex) (1)(2)	2(3)		3		3		3		3	
	I^2SF (full-duplex)	1		1		1		1		1	
	USART/UART	5/2(4)		5/2(4)		5/2(4)		6/2		6/2	
	CAN	1		1		1		1		1	
	OTGHS	1		1		1		1		1	
	OTGFS	1		1		1		1		1	
	IRTMR	1		1		1		1		1	
Analog	12-bit ADC numbers/ external channels	1		1		1		1		1	
		10		10		10		16		16	
GPIO		25		37		37		53		53	
Operating temperature		-40 °C to +105 °C									
Packages		QFN32 4 x 4 mm		QFN48 6 x 6 mm		LQFP48 7 x 7 mm		LQFP64 7 x 7 mm		LQFP64 10 x 10 mm	

(1) Half-duplex I^2S share the same pin with SPI.
(2) Two half-duplex I^2S can be combined to support full-duplex I^2S mode.
(3) For QFN32 package, only SPI1/I^2S1 and SPI3/I^2S3 are supported.
(4) For 48-pin packages and smaller, UART8 is not available, and USART6 can only be used as UART for no CK pinout.

Table 4. AT32F402 features and peripheral counts

Part number		AT32F402xxU7-4		AT32F402xxU7		AT32F402xxT7		AT32F402xxT7-7		AT32F402xxT7	
		KB	KC	CB	CC	CB	CC	RB	RC	RB	RC
Frequency (MHz)		216									
Internal Flash (KB)		128	256	128	256	128	256	128	256	128	256
SRAM (KB)		64+6	96+6	64+6	96+6	64+6	96+6	64+6	96+6	64+6	96+6
QSPI		1		1		1		1		1	
Timers	Advanced	1		1		1		1		1	
	32-bit general-purpose	1		1		1		1		1	
	16-bit general-purpose	7		7		7		7		7	
	Basic	2		2		2		2		2	
	SysTick	1		1		1		1		1	
	WDT	1		1		1		1		1	
	WWDT	1		1		1		1		1	
	ERTC	1		1		1		1		1	
Communication interfaces	I^2C	3		3		3		3		3	
	SPI(1)	2(3)		3		3		3		3	
	I^2S (half-duplex) (1)(2)	2(3)		3		3		3		3	
	I^2SF (full-duplex)	1		1		1		1		1	
	USART/UART	5/2(4)		5/2(4)		5/2(4)		6/2		6/2	
	CAN	1		1		1		1		1	
	OTGHS	-		-		-		-		-	
	OTGFS	1		1		1		1		1	
	IRTMR	1		1		1		1		1	
Analog	12-bit ADC numbers/ external channels	1		1		1		1		1	
		10		10		10		16		16	
GPIO		28		40		40		56		56	
Operating temperatures		-40 °C to +105 °C									
Packages		QFN32 4 x 4 mm		QFN48 6 x 6 mm		LQFP48 7 x 7 mm		LQFP64 7 x 7 mm		LQFP64 10 x 10 mm	

(1) Half-duplex I^2S shares the same pin with SPI.
(2) Two half-duplex I^2S can be combined to support full-duplex I^2S mode.
(3) For QFN32 package, only SPI1/I^2S1 and SPI3/I^2S3 are supported.
(4) For 48-pin packages and smaller, UART8 is not available, and USART6 can only be used as UART for no CK pinout.

2 Functionality overview

2.1 ARM®Cortex®-M4 with FPU

The ARM®Cortex®-M4 processor is the latest generation of ARM® processor for embedded systems. It is a 32-bit RISC high-performance processor that features exceptional code efficiency, outstanding computing power and advanced response to interrupts. The processor supports a set of DSP instructions that enable efficient signal processing and complex algorithm execution. Its single-precision FPU (floating point unit) speeds up floating point calculations while avoiding saturation.

2.2 Memory

2.2.1 Internal Flash memory

Up to 256 Kbytes of embedded Flash is available for storing programs and data. Any part of the embedded Flash memory can be protected by sLib (security library), a security area that is code-executable only but non-readable. The “sLib” is a mechanism designed to protect the intelligence of solution venders and facilitate the second-level development by customers.

There is another 20-Kbyte boot memory in which the bootloader is stored. If it is not needed, this boot memory can be used as a general instruction/data memory (one-time programmable) instead.

A User System Data block is available for hardware configurations such as access/erase/write protection, watchdog self-enable and SRAM parity check. User System Data allows the independent configuration of Flash memory erase/write and access protection. There are two levels of memory access protection: low-level protection and high-level protection.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.2.3 SRAM

It is possible to configure the on-chip SRAM as 102 Kbytes with no parity check (by default) or 96 Kbytes (the first 48 Kbytes with parity check function), which is accessible at CPU clock speed with 0 wait state (for read/write access).

2.2.4 Quad SPI interface (QSPI)

The AT32F405/402 devices embed a quad SPI interface (QSPI). It is a specialized communication interface to be connected with single, dual or quad SPI Flash memories, or SPI RAM. It can operate in indirect mode (all operations are started by writing to corresponding registers), status polling mode or memory-mapped mode. Up to 256 MB external Flash memory or RAM can be mapped onto the device address space.

Byte access, half-word access and word access types are all supported for QSPI. It also supports XIP operation — execute in place operation. Operation code and frame format are programmable.

2.3 Interrupts

2.3.1 Nested vectored interrupt controller (NVIC)

The AT32F405/402 series embed a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.2 External interrupts (EXINT)

The external interrupt controller (EXINT), which is connected directly to NVIC, consists of 22 edge detectors for generating interrupt requests. Each interrupt line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connects up to 16 GPIOs.

2.4 Power control (PWC)

2.4.1 Power supply schemes

- V_{DD} = 2.4~3.6 V: power supply for GPIOs, ERTC, external 32 kHz crystal (LEXT), battery-powered register (BPR) and the internal blocks such as voltage regulator (LDO), provided externally via V_{DD} pins
- V_{DDA} = 2.4~3.6 V: power supply for ADC. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively, provided externally via V_{DDA} pins

2.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR) and low-voltage reset (LVR) circuitry. It is always active and allows proper operation starting from 2.4 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}), without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt is generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.4.3 Voltage regulator (LDO)

The LDO has three operating modes: normal, low-power, and power down.

- Normal mode: used in Run/Sleep mode or in Deepsleep mode;
- Low-power mode: used in Deepsleep mode;
- Power down mode: used in Standby mode. The regulator LDO output is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

This LDO operates in normal mode after reset.

2.4.4 Low-power modes

The AT32F405/402 series support three low-power modes:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Deepsleep mode**

  Deepsleep mode achieves low-power consumption while holding the content of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock and the HEXT crystal. The voltage regulator (LDO) can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm, wakeup, tamper, time stamp event, OTGHS or OTGFS wakeup signal.

- **Standby mode**

  The Standby mode is used to acquire the lowest power consumption. The internal LDO is switched off so that the entire LDO power domain is powered off. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for ERTC and BPR registers and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUPx pin, or an ERTC alarm/wakeup/tamper/time stamp occurs.

Note: The ERTC and the corresponding clock sources are not stopped by entering Deepsleep or Standby mode. WDT depends on the User System Data settings.

2.5 Boot modes

At startup, BOOT0 pin and nBOOT1 bit in the User System Data are used to select one of three boot options:

- Boot from Flash memory;
- Boot from boot memory;
- Boot from embedded SRAM.

The bootloader is stored in the boot memory. It is used to reprogram the Flash memory through USART1, USART2, USART3, OTGHS1, OTGFS1, I²C1, I²C2, I²C3, CAN1 or SPI1. Of them, OTGHS1 must be used in conjunction with 12 MHz HEXT, and OTGFS1 supports crystal-less operation mode. CAN1 must be used in conjunction with one of the following HEXT oscillators: 4, 6, 8, 12, 14.7456, 16, 20, 24 or 25 MHz. *Table 5* provides the pin configurations for bootloader.

Table 5. AT32F405 series bootloader pin configurations

Peripherals	Part number	Pin
USART1	AT32F405KxU7-4	Not support
	Other part numbers	PA9: USART1_TX PA10: USART1_RX
USART2	All part numbers	PA2: USART2_TX PA3: USART2_RX
USART3	AT32F405RxT7, AT32F405RxT7-7	PC10: USART3_TX PC11: USART3_RX
	Other part numbers	Not support
OTGHS1	All part numbers	OTGHS1_D- OTGHS1_D+
OTGFS1	All part numbers	PA11: OTGFS1_D- PA12: OTGFS1_D+
I²C1	All part numbers	PB6: I2C1_SCL PB7: I2C1_SDA
I²C2	AT32F405KxU7-4	Not support
	Other part numbers	PB10: I2C2_SCL PB3: I2C2_SDA
I²C3	AT32F405KxU7-4	Not support
	Other part numbers	PA8: I2C3_SCL PB4: I2C3_SDA
CAN1	AT32F405KxU7-4	Not support
	Other part numbers	PB8: CAN1_RX PB9: CAN1_TX
SPI1	All part numbers	PA4: SPI1_CS PA5: SPI1_SCK PA6: SPI1_MISO PA7: SPI1_MOSI

Table 6. AT32F402 series bootloader pin configurations

Peripherals	Part number	Pin
USART1	All part numbers	PA9: USART1_TX PA10: USART1_RX
USART2	All part numbers	PA2: USART2_TX PA3: USART2_RX
USART3	AT32F402RxT7, AT32F402RxT7-7	PC10: USART3_TX PC11: USART3_RX or PB10: USART3_TX PB11: USART3_RX
	AT32F402CxT7, AT32F402CxU7	PB10: USART3_TX PB11: USART3_RX
	Other part numbers	Not support
OTGFS1	All part numbers	PA11: OTGFS1_D- PA12: OTGFS1_D+
I^2C1	All part numbers	PB6: I2C1_SCL PB7: I2C1_SDA
I^2C2	AT32F402KxU7-4	Not support
	Other part numbers	PB10: I2C2_SCL PB3: I2C2_SDA
I^2C3	All part numbers	PA8: I2C3_SCL PB4: I2C3_SDA
CAN1	AT32F402KxU7-4	Not support
	Other part numbers	PB8: CAN1_RX PB9: CAN1_TX
SPI1	All part numbers	PA4: SPI1_CS PA5: SPI1_SCK PA6: SPI1_MISO PA7: SPI1_MOSI

2.6 Clocks

The internal 48 MHz clock (HICK) divided by 6 (that is 8 MHz) is selected as the default CPU clock after any reset. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system takes the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are available to allow the configuration of the AHB and the APB (APB1 and APB2) frequencies. The maximum frequency of the AHB/APB2 domains is 216 MHz, and APB1 120 MHz. The maximum allowed frequency of the AHB domain is 120 MHz while accessing CRM_BPDC register and CRM_CTRLSTS register.

The AT32F405/402 series embed an automatic clock calibration (ACC) block, which calibrates the internal 48 MHz HICK, assuring the most precise accuracy of the HICK in the full range of the operating temperatures.

2.7 General-purpose inputs / outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain with or without pull-up or pull-down), as input (floating with or without pull-up or pull-down), or as multiplexed functions. Most of the GPIO pins are shared with digital or analog multiplexed functions. All GPIOs are high current-capable.

The GPIO's configuration can be locked if needed, in order to avoid false writing to the GPIO's registers by following a specific sequence.

2.8 Direct Memory Access Controller (DMA)

AT32F405/402 features two general-purpose DMA ports (7-channel DMA1 and 7-channel DMA2). They are able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. These DMA channels can be connected to peripherals for flexible mapping.

The DMA controller supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software, and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI/I^2S (half-duplex), I^2SF (full-duplex), I^2C, USART/UART, advanced, general-purpose, and basic timers (TMR), ADC and QSPI.

2.9 Timers (TMR)

The AT32F405/402 series include an advanced timer, up to eight general-purpose timers, two basic timers and a SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

Table 7. Timer feature comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output
Advanced	TMR1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TMR2	16-bit or 32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR3 TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR9	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	2	2
	TMR10 TMR11 TMR13 TMR14	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	1	1
Basic	TMR6 TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

2.9.1 Advanced timer (TMR1)

The advanced timer (TMR1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable dead-time insertion. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-cycle mode output

If configured as a standard 16-bit timer, it has the same features as that of the TMRx timer. If configured as a 16-bit PWM generator, it boasts full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen, and the PWM outputs are disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMRs that have the same architecture. Thus, the advanced timer can work together with the general-purpose TMR timers via the link feature for synchronization or event chaining.

2.9.2 General-purpose timers (TMR2~4, TMR9~11 and TMR13~14)

Up to eight synchronizable general-purpose timers are available in the AT32F405/402.

- **TMR2, TMR3 and TMR4**

  The TMR2 timer is based on a 32-bit auto-reload upcounter/downcounter and a 16-bit prescaler. TMR3 and TMR4 timers are based on a 16- bit auto-reload upcounter/downcounter and a 16-bit prescaler. They can offer four independent channels on the largest packages. Each channel can be used for input capture/output compare, PWM or one-cycle mode output.

  These general-purpose timers can work with the advanced timer via the link feature for synchronization or event chaining. In debug mode, counters can be frozen. Any of these general-purpose timers can be used for the generation of PWM output. Each timer has its individual DMA request mechanism. They are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors. The counter can be frozen in debug mode.

- **TMR9**

  TMR9 is based on a 16-bit auto-reload upcounter/downcounter, a 16-bit prescaler, and two independent channels and two complementary channels for input capture/output compare, PWM, or one-cycle mode output. It can be synchronized with full-featured general-purpose timers. TMR9 can also be used as a simple timer. In debug mode, counter can be frozen. TMR9 has its separate DMA request generation mechanism.

- **TMR10, TMR11, TMR13 and TMR14**

  These timers are based on a 16-bit auto-reload upcounter/downcounter, a 16-bit prescaler, and one independent channel and one complementary channel for input capture/output compare, PWM, or one-cycle mode output. They can be synchronized with full-featured general-purpose timers. They can also be used as simple timers. In debug mode, counters can be frozen. Each of these timers has its separate DMA request mechanism.

2.9.3 Basic timers (TMR6 and TMR7)

Both timers are mainly used as generic 16-bit time base.

2.9.4 SysTick timer

This timer is dedicated to real-time operating systems, but it could also be used as a standard downcounter. Its features include:

- A 24-bit downcounter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HICK or HICK/8)

2.10 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabled or not through the User System Data. The counter can be frozen in debug mode.

2.11 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock. It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.12 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- 20x 32-bit battery powered registers (BPRs)

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Support sub-seconds value in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms and periodic interrupts wake up Deepsleep or Standby mode.
- To compensate quartz crystal inaccuracy, ERTC can be calibrated via a 512 Hz external output.

There are two alarm registers used to generate an alarm at a specific time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, week day and date.

A prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 80 bytes of user application data. Battery powered registers are not reset by a system or power reset, nor when the device is woken up from the Standby mode.

2.13 Communication interfaces

2.13.1 Serial peripheral interface (SPI)

There are up to three SPIs able to communicate at up to 32 Mbits/s in slave and master modes, in full-duplex and half-duplex modes. The prescaler can be used to generate multiple master mode frequencies. The frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD card/MMC/SDHC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master and slave modes.

2.13.2 Half-duplex/full-duplex inter-integrated sound interface (I^2S/I^2SF)

Three standard I^2S interfaces (multiplexed with SPI) are available, which can be operated in master or slave mode. These interfaces can be configured to operate with 16/24/32-bit resolution, as input or output channels. Audio sampling frequencies ranges from 8 kHz up to 192 kHz. When I^2S is configured in master mode, the master clock can be output at 256 times the sampling frequency.

All I^2Ss can be served by the DMA controller.

In addition, any two of I^2S interfaces in half-duplex mode can be combined (through hardware) to achieve full-duplex communication function, while the remaining interface can still operate independently or used as a SPI.

In addition to half-duplexed I^2S interface, the AT32F405/402 series offer a separate full-duplexed I^2S interface (I^2SF), which can be configured to operate with 16/24/32-bit resolution, as input or output channels. When the full-duplex I^2S interface is configured in master mode, the master clock can be output at 256 times the sampling frequency.

The main input clock source of I^2SF interface can be system clock, PLL output clock, 48 MHz HICK and external input clock. More precise audio frequency can be achieved by setting the main input clock of I^2SF interface.

2.13.3 Universal synchronous / asynchronous receiver transmitters (USART)

The AT32F405/402 series embed six universal synchronous/asynchronous receiver transmitters (USART1~6) and two universal asynchronous transceivers (UART7~8).

These eight interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, LIN Master/Slave capability. Most USART interfaces provide hardware management of the CTS and RTS signals, RS485 drive enable signal, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All interfaces can be served by the DMA controller.

USART1 and USART6 are able to communicate at up to 13.5 Mbit/s, and others at up to 7.5 Mbit/s.

Table 8. USART/UART comparison

USART/UART feature	USART1	USART2	USART3	USART4	USART5	USART6	UART7	UART8
Modem with hardware flow control	Yes	Yes	Yes	Yes	-	-	-	-
Continuous communication using DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multiprocessor communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Synchronous mode	Yes	Yes	Yes	Yes	Yes	Yes	-	-
Smart card mode	Yes	Yes	Yes	Yes	Yes	Yes	-	-
Single-wire half-duplex communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IrDA SIR ENDEC	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LIN mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
TX/RX swap	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
RS-485 drive enable	Yes	Yes	Yes	Yes	Yes	Yes	-	-

2.13.4 Inter-integrated-circuit interface (I^2C)

Three I^2C bus interfaces can operate in multi-master and slave modes. They can support standard mode (max. 100 kHz), fast mode (max. 400 kHz) and fast mode plus (max. 1 MHz). Some GPIOs provide ultra-high sink current of 20 mA.

They support 7-bit/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.13.5 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages, and 14 scalable filter banks. It also has dedicated 256 bytes of SRAM, which is not shared with any other peripherals.

To guarantee CAN transmission quality, the CAN 2.0 protocol states that its clock source must come from the HEXT-based PLL clock.

2.13.6 Universal serial bus On-The-Go high-speed (OTGHS)

This peripheral applies to AT32F405 series only.

The AT32F405 series embeds one OTG high-speed (up to 480 Mb/s) device/host peripherals with integrated transceivers (PHY). It offers dedicated OTGHS_D+, OTGHS_D-, and OTGHS_R pin without sharing with GPIO or other functions. The OTGHS controller has software-configurable endpoint settings and supports suspend/resume.

The OTGHSPHY controller requires a dedicated 480 MHz clock that is generated by a PLL connected to HEXT 12 MHz oscillator. Internal clock sources or other external oscillators are not supported.

OTGHS module has the major features as follows:

- Dedicated 4096 bytes of buffer (not shared with any other peripherals)
- 8 IN + 8 OUT endpoints (including endpoint 0, device mode)
- 16 channels (host mode)
- DMA controller
- SOF and OE output
- In accordance with the USB 2.0 Specification, the transfer speeds supported are:
  - Host mode: High-speed, full-speed and low-speed
  - Device mode: High-speed and full-speed

2.13.7 Universal serial bus On-The-Go full-speed (OTGFS)

The AT32F405/402 series embed one OTG full-speed (12 Mb/s) device/host peripherals with integrated transceivers (PHY). It has software-configurable endpoint settings and supports suspend/resume. The OTGFS controller requires a dedicated 48 MHz clock. In master mode, such clock must be generated by a HEXT-based PLL. In device mode, this clock can be provided by 48 MHz HICK directly.

OTGFS has the major features as follows:

- Dedicated 1280 bytes of buffer (not shared with any other peripherals)
- 8 IN + 8 OUT endpoints (endpoint 0 included, device mode)
- 16 channels (host mode)
- SOF and OE output
- In accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - Host mode: full-speed and low-speed
  - Device mode: full-speed

2.13.8 Infrared transmitter (IRTMR)

The AT32F405/402 series offer an infrared transmitter solution. The solution is based on the internal connection between TMR10, USART1, or USART2 and TMR11. The TMR11 is used to provide carrier frequency, while TMR10, USART1, or USART2 provides the main signal to be sent. The Infrared output signal is available on PB9 or PA13.

To generate infrared remote control signals, TMR10 channel 1 and TMR11 channel 1 must be correctly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

2.14 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

2.15 Analog-to-digital converter (ADC)

A 12-bit 2 MSPS analog-to-digital converter (ADC) is embedded in AT32F405/402 series. It shares up to 16 external channels and two internal channels. These two internal channels are connected to an internal temperature sensor (V_{TS}) and internal reference voltage (V_{REFINT}), respectively. The ADC controller offers a configurable oversampling method by 2 to 256, up to 16-bit resolution equivalent. It supports single mode or sequential mode for conversion. In sequential mode, each trigger starts ADC conversion on a selected group of analog channels.

The ADC can be served by the DMA controller.

A voltage monitor feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

Events generated by general-purpose timers (TMRx) and advanced timer (TMR1) can be connected with ADC regular channels and preempted group, respectively. It is possible to synchronize ADC conversion with clocks through application program.

2.15.1 Temperature sensor (V_{TS})

The temperature sensor generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel that is used to convert the sensor output voltage into a digital value.

The offset of this line varies from chip to chip due to process variation. The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

2.15.2 Internal reference voltage (V_{INTRV})

The internal reference voltage (V_{INTRV}) provides a stable voltage source for ADC. The V_{INTRV} is internally connected to the ADC1_IN17 input channel.

2.16 Serial wire debug (SWD) / serial wire output (SWO)

The ARM®SWD interface is embedded in the AT32F405/402 series. It is a serial wire debug port that enables either a serial wire debug to be connected to the target for programming and debugging purposes. In addition, the SWO feature is available for asynchronous tracing in debug mode.

3 Pin functional definitions

The AT32F405 series is largely pin-to-pin compatible with the AT32F402 series except for the following several pins marked in blue.

Figure 1. AT32F405 LQFP64 pinout

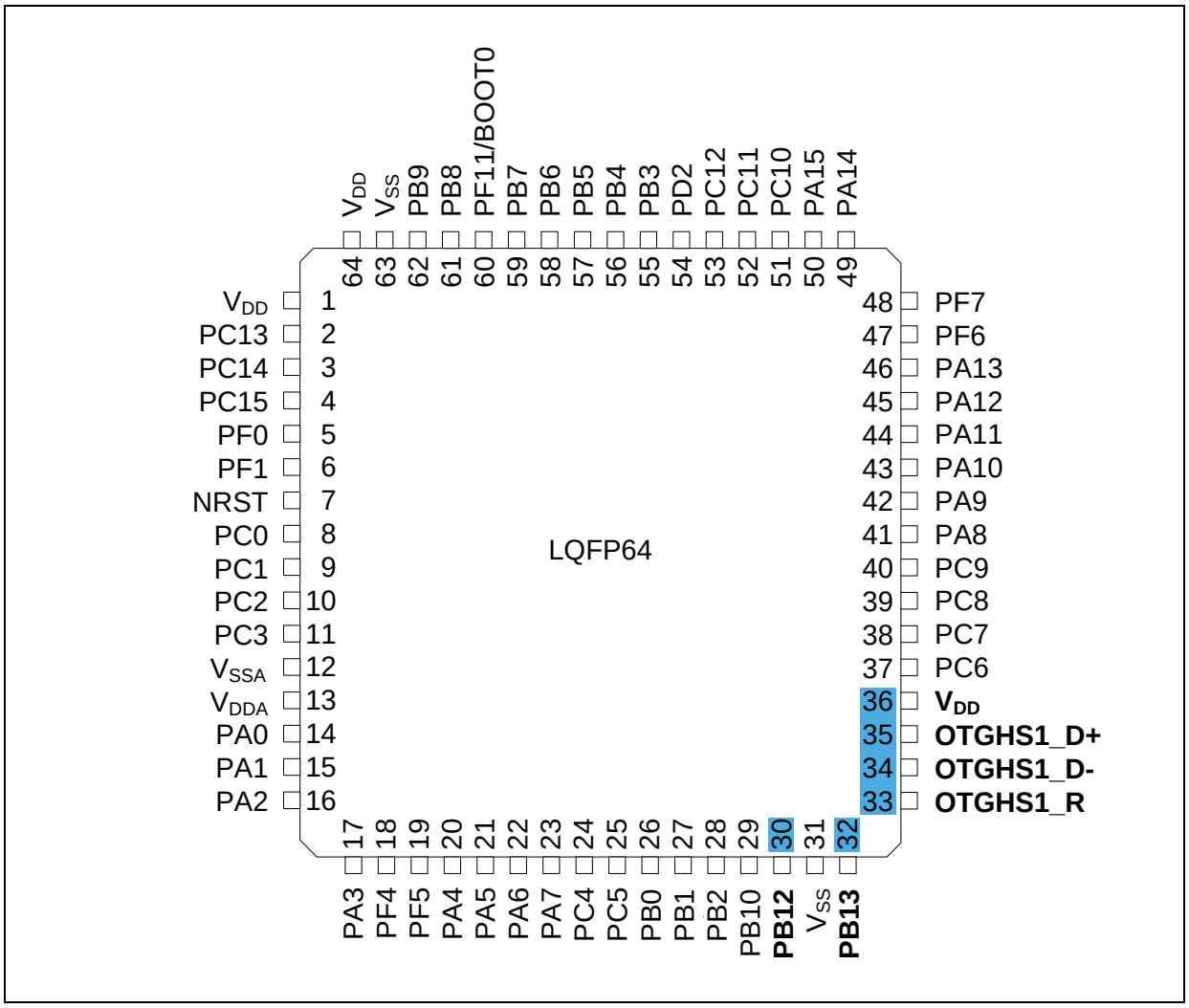


Figure 2. AT32F402 LQFP64 pinout

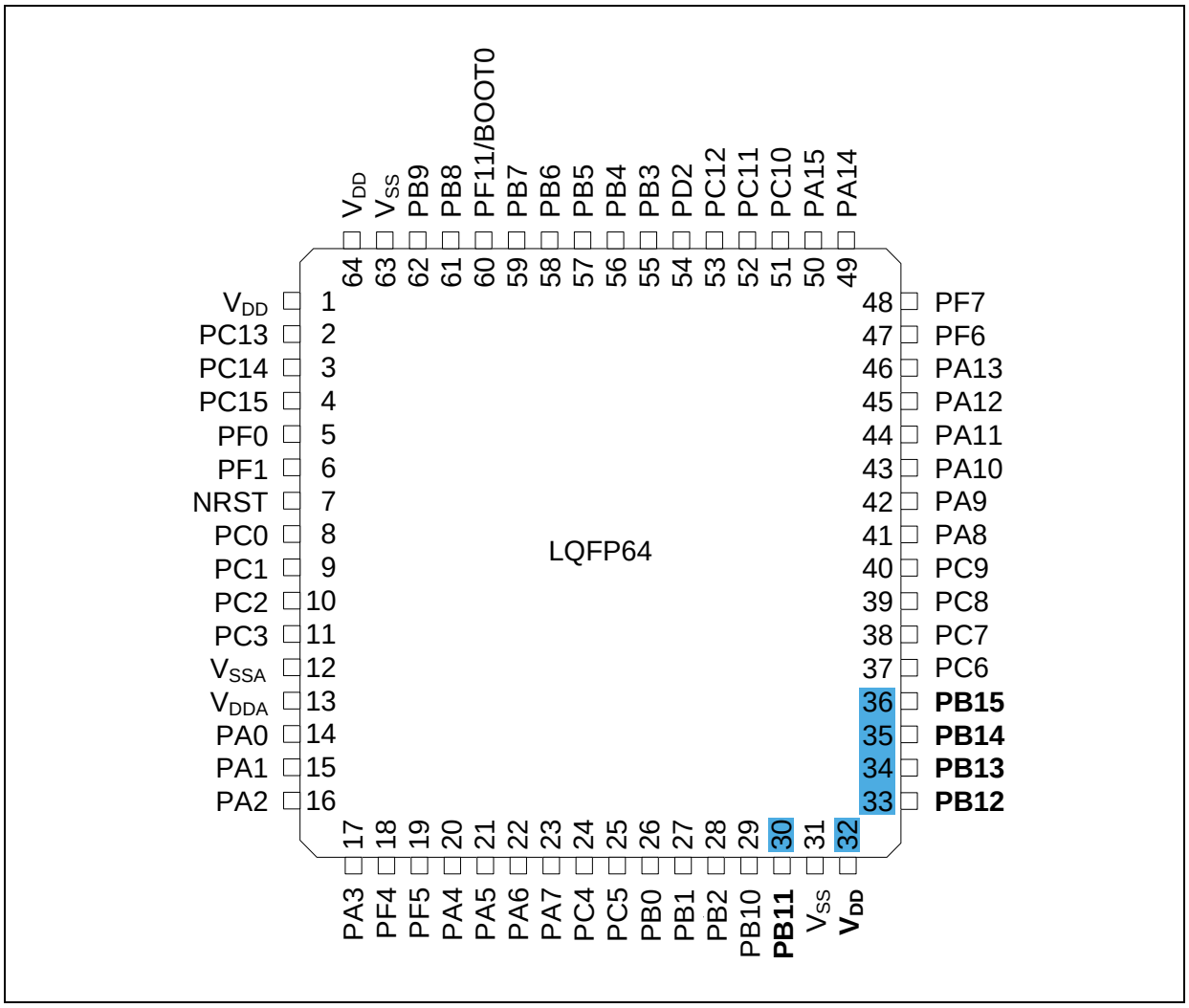


Figure 3. AT32F405 LQFP48 pinout

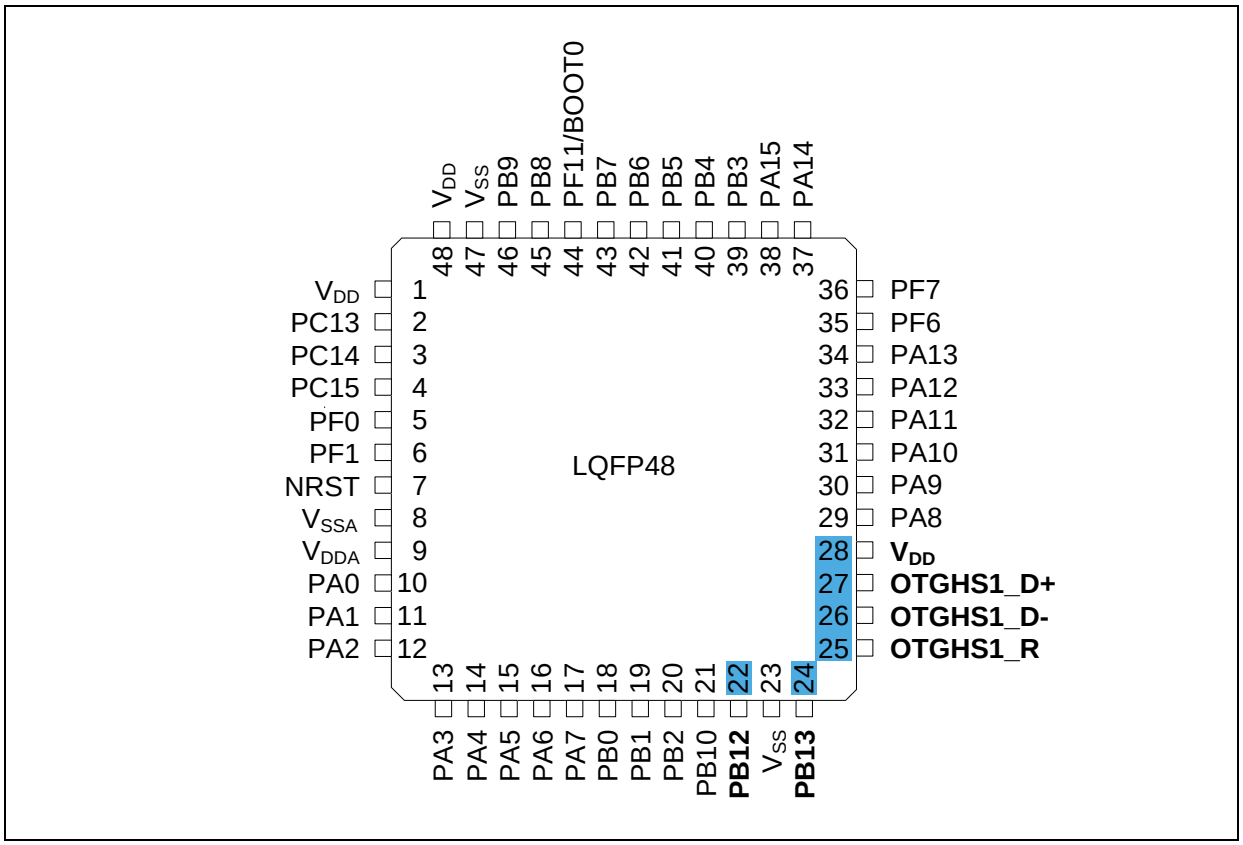


Figure 4. AT32F402 LQFP48 pinout

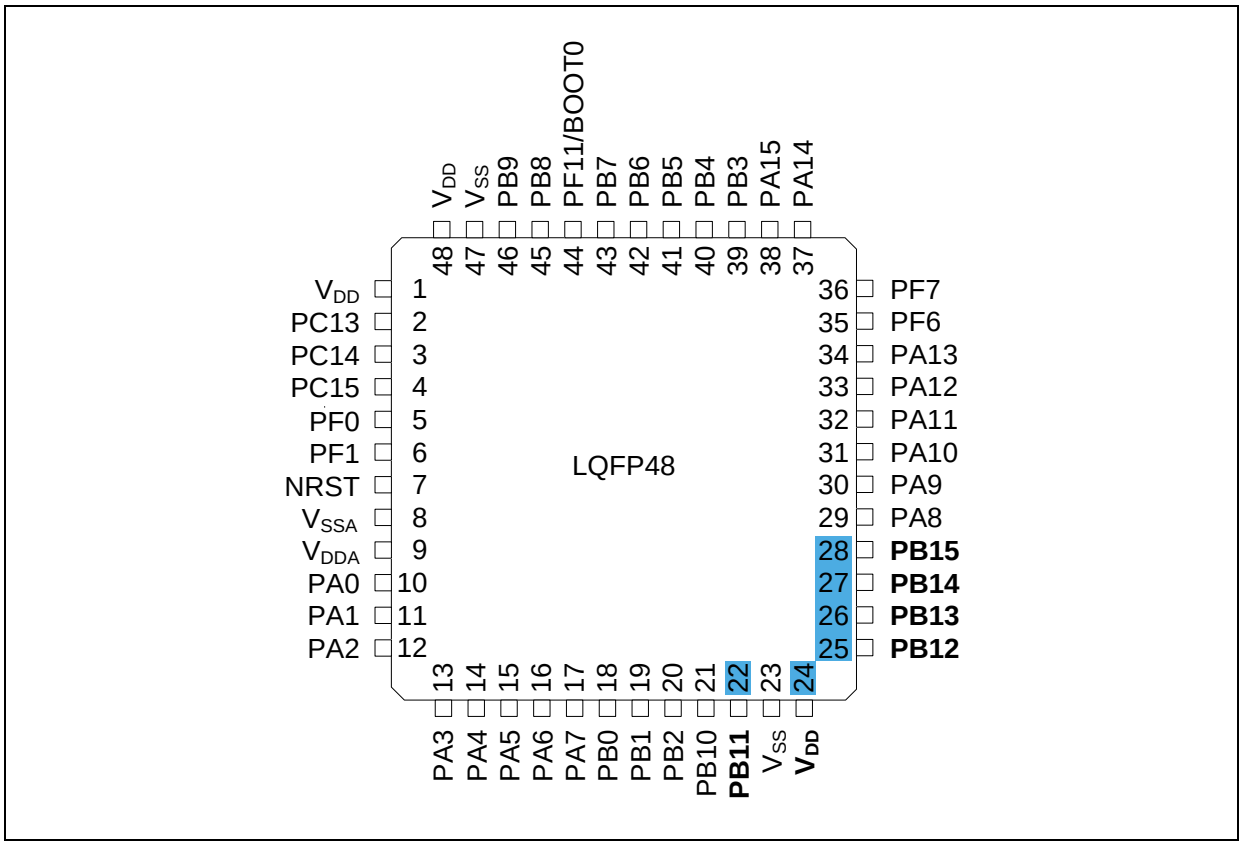


Figure 5. AT32F405 QFN48 pinout

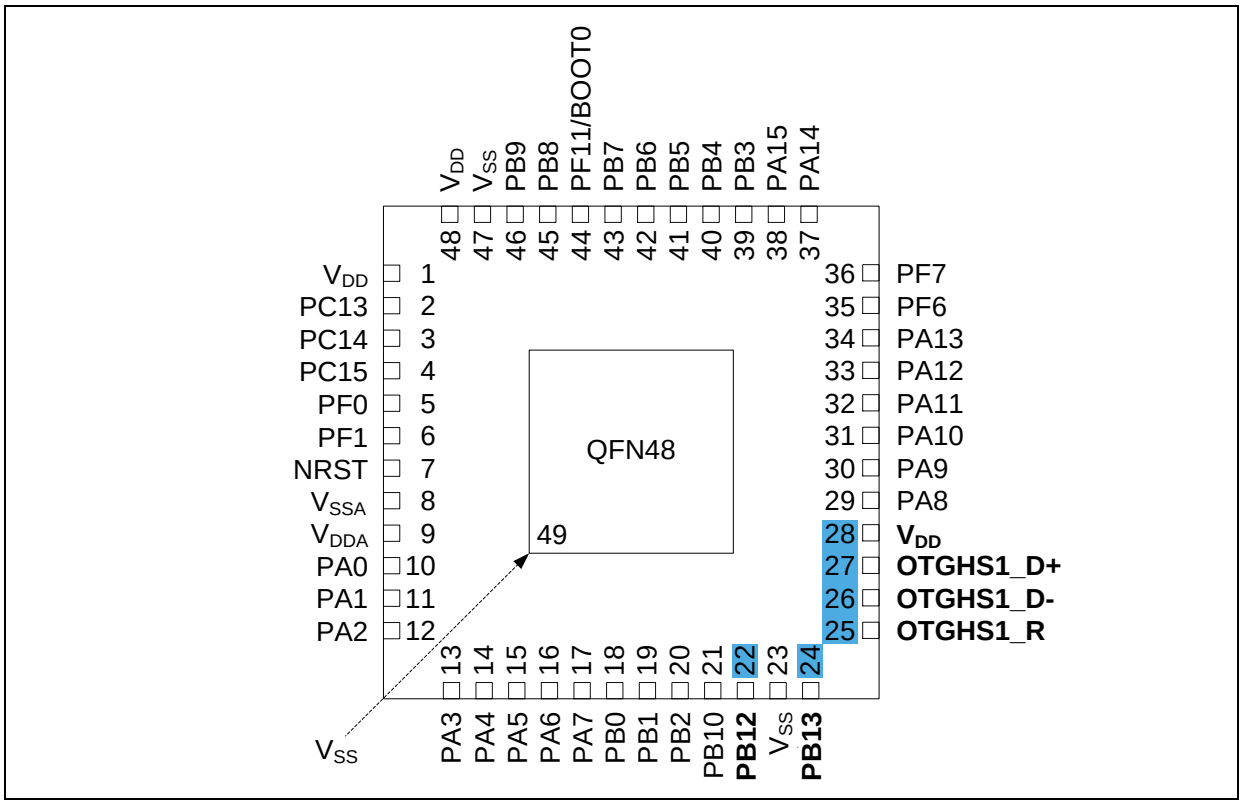


Figure 6. AT32F402 QFN48 pinout

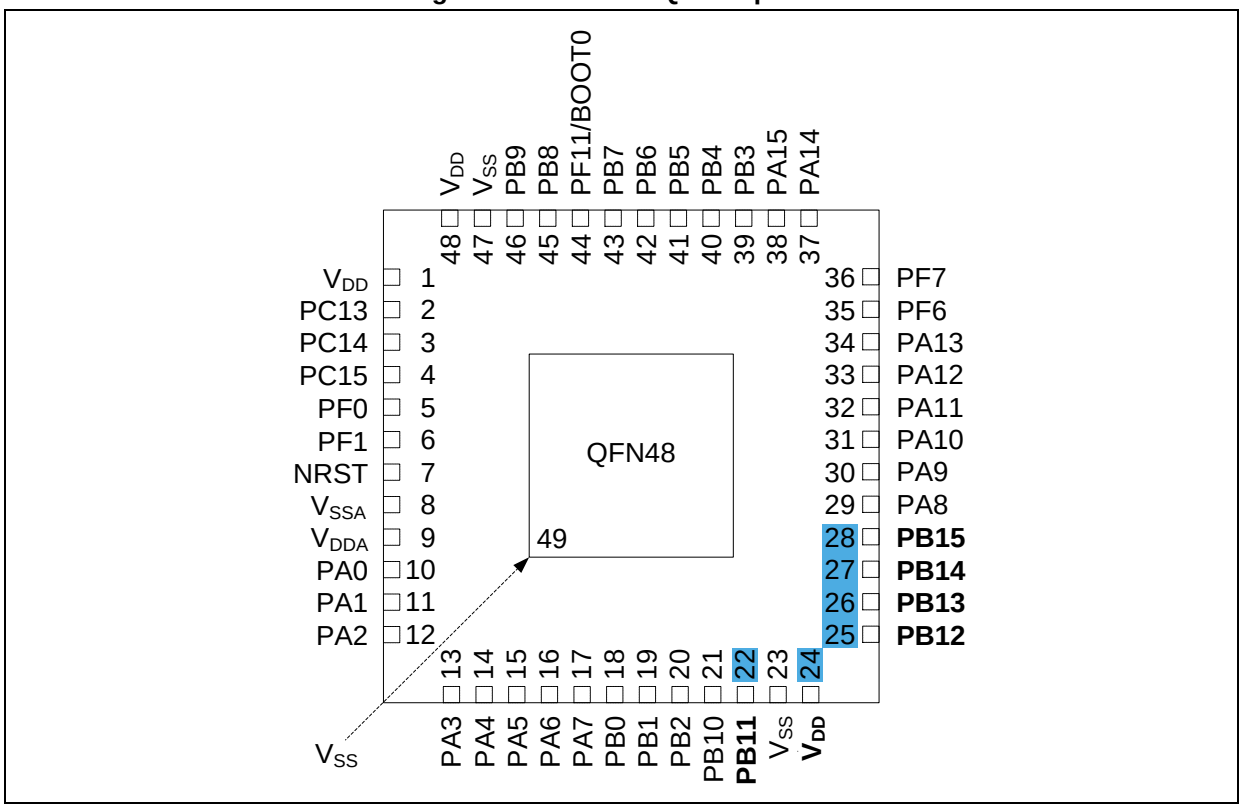


Figure 7. AT32F405 QFN32 pinout

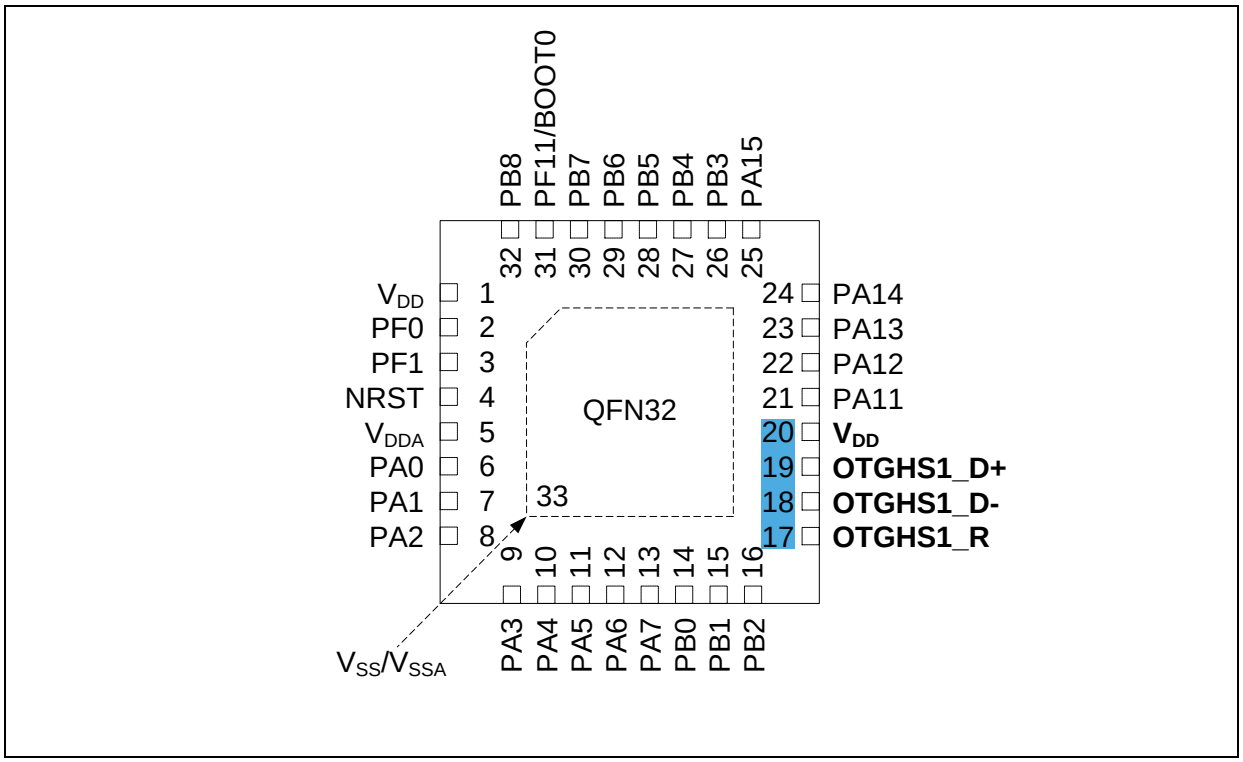
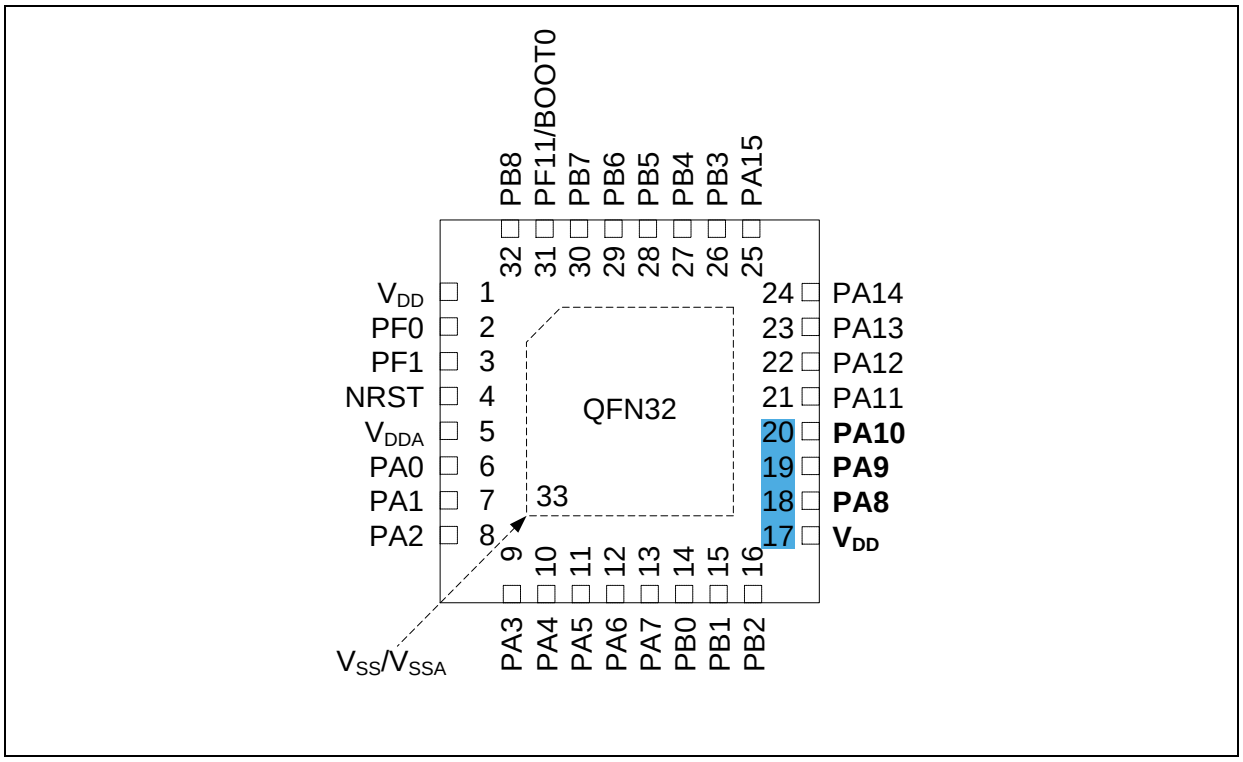


Figure 8. AT32F402 QFN32 pinout



The table below is the pin definition of the AT32F405/402. “-” represents that there is no such pinout on the related package. Unless descriptions in () under pin name, the functions during reset and after reset are the same as those of the actual pin name. Unless otherwise specified, all GPIOs are set as input floating during reset and after reset. Pin multiplexed functions are selected through GPIOx_MUXx registers and the additional functions are directly selected/enabled through peripheral registers.

Table 9. AT32F405/402 series pin definitions

Pin number						Pin name (function after reset)	Type (1)	GPIO level(2)	Multiplexed functions (3)	Additional functions
AT32F405			AT32F402							
QFN32	LQFP48/ QFN48	LQFP64	QFN32	LQFP48/ QFN48	LQFP64					
-	1	1	-	1	1	V_{DD}	S	-	Digital power supply	
-	2	2	-	2	2	PC13	I/O	FT	-	ERTC_OUT / TAMP1 / WKUP2
-	3	3	-	3	3	PC14	I/O	TC	-	LEXT_IN
-	4	4	-	4	4	PC15	I/O	TC	-	LEXT_OUT
2	5	5	2	5	5	PF0	I/O	TC	TMR1_CH1 / I2C1_SDA	HEXT_IN
3	6	6	3	6	6	PF1	I/O	TC	TMR1_CH2C / I2C1_SCL / SPI2_CS / I2S2_WS	HEXT_OUT
4	7	7	4	7	7	NRST	I/O	R	Device reset input/internal reset output (active low)	
-	-	8	-	-	8	PC0	I/O	FTa	I2C3_SCL / I2C1_SCL / USART6_TX / UART7_TX	ADC1_IN10
-	-	9	-	-	9	PC1	I/O	FTa	I2C3_SDA / SPI3_MOSI / I2S3_SD / SPI2_MOSI / I2S2_SD / I2C1_SDA / USART6_RX / UART7_RX	ADC1_IN11
-	-	10	-	-	10	PC2	I/O	FTa	SPI2_MISO / I2S2_MCK / I2S_SDEXT / UART8_TX	ADC1_IN12
		11			11	PC3	I/O	FTa	SPI2_MOSI / I2S2_SD / UART8_RX	ADC1_IN13
-	8	12	-	8	12	V_{SSA}	S	-	Analog ground	
5	9	13	5	9	13	V_{DDA}	S	-	Analog power supply	
6	10	14	6	10	14	PA0	I/O	FTa	TMR2_CH1 / TMR2_EXT / TMR9_CH2C / I2C2_SCL / USART2_RX / USART2_CTS / USART4_TX /	ADC1_IN0 / TAMP2 / WKUP1
7	11	15	7	11	15	PA1	I/O	FTa	TMR2_CH2 / TMR9_CH1C / I2C2_SDA / I2C1_SMBA / I2SF5_SD / USART2_RTS_DE / USART4_RX / QSPI1_IO3	ADC1_IN1
8	12	16	8	12	16	PA2	I/O	FTa	TMR2_CH3 / TMR9_CH1 / I2SF5_CKIN / USART2_TX / QSPI1_CS	ADC1_IN2
9	13	17	9	13	17	PA3	I/O	FTa	TMR2_CH4 / TMR9_CH2 / I2S2_MCK / USART2_RX	ADC1_IN3
-	-	18	-	-	18	PF4	I/O	FT	TMR2_CH1 / I2C1_SDA	-
-	-	19	-	-	19	PF5	I/O	FT	TMR2_CH2 / I2C1_SCL	-

Pin number						Pin name (function after reset)	Type (1)	GPIO level(2)	Multiplexed functions (3)	Additional functions
AT32F405			AT32F402							
QFN32	LQFP48/ QFN48	LQFP64	QFN32	LQFP48/ QFN48	LQFP64					
10	14	20	10	14	20	PA4	I/O	FTa	I2C1_SCL / SPI1_CS / I2S1_WS / SPI3_CS / I2S3_WS / USART2_CK / USART6_TX / TMR14_CH1 / OTGHS1_SOF	ADC1_IN4
11	15	21	11	15	21	PA5	I/O	FTa	TMR2_CH1 / TMR2_EXT / SPI1_SCK / I2S1_CK / USART3_CK / USART3_RX / USART6_RX / TMR13_CH1C	ADC1_IN5
12	16	22	12	16	22	PA6	I/O	FTa	TMR1_BRK / TMR3_CH1 / SPI1_MISO / I2S1_MCK / I2S2_MCK / USART3_CTS / USART3_RX / TMR13_CH1 / QSPI1_IO0 / QSPI1_IO2	ADC1_IN6
13	17	23	13	17	23	PA7	I/O	FTa	TMR1_CH1C / TMR3_CH2 / I2C3_SCL / SPI1_MOSI / I2S1_SD / USART3_TX / TMR14_CH1 / QSPI1_IO1	ADC1_IN7
-	-	24	-	-	24	PC4	I/O	FTa	TMR9_CH1 / I2S1_MCK / USART3_TX / TMR13_CH1 / QSPI1_IO2	ADC1_IN14
-	-	25	-	-	25	PC5	I/O	FTa	TMR9_CH2 / I2C1_SMBA / USART3_RX / TMR13_CH1C / QSPI1_IO3	ADC1_IN15
14	18	26	14	18	26	PB0	I/O	FTa	TMR1_CH2C / TMR3_CH3 / SPI1_MISO / I2S1_MCK / SPI3_MOSI / I2S3_SD / USART2_RX / USART3_CK / QSPI1_IO0 / I2SF5_CK	ADC1_IN8
15	19	27	15	19	27	PB1	I/O	FTa	TMR1_CH3C / TMR3_CH4 / SPI1_MOSI / I2S1_SD / SPI2_SCK / I2S2_CK / USART2_CK / USART3_RTS_DE / TMR14_CH1 / QSPI1_SCK / I2SF5_WS	ADC1_IN9
16	20	28	16	20	28	PB2	I/O	FT	TMR2_CH4 / TMR3_EXT / I2C3_SMBA / SPI3_MOSI / I2S3_SD / TMR14_CH1C / QSPI1_SCK	-
-	21	29	-	21	29	PB10	I/O	FTf	TMR2_CH3 / I2C2_SCL / SPI2_SCK / I2S2_CK / I2S3_MCK / USART3_TX / QSPI1_IO1 / QSPI1_CS	-
-	-	-	-	22	30	PB11	I/O	FT	TMR2_CH4 / I2C2_SDA / I2SF5_CKIN / USART3_RX / TMR13_BRK / QSPI1_IO0	-
-	22	30	-	-	-	PB12	I/O	FT	TMR1_BRK / I2C2_SMBA / SPI2_CS / I2S2_WS / SPI3_SCK / I2S3_CK / USART3_CK / OTGHS1_ID / I2SF5_WS	-

Pin number						Pin name (function after reset)	Type (1)	GPIO level(2)	Multiplexed functions (3)	Additional functions
AT32F405			AT32F402							
QFN32	LQFP48/ QFN48	LQFP64	QFN32	LQFP48/ QFN48	LQFP64					
-	23	31	-	23	31	V_{SS}	S	-	Digital ground	
-	-	-	17	24	32	V_{DD}	S	-	Digital power supply	
-	-	-	-	25	33	PB12	I/O	FT	TMR1_BRK / I2C2_SMBA / SPI2_CS / I2S2_WS / SPI3_SCK / I2S3_CK / USART3_CK / I2SF5_WS	-
-	24	32	-	26	34	PB13	I/O	FT	CLKOUT / TMR1_CH1C / I2C3_SMBA / SPI2_SCK / I2S2_CK / I2SF5_CK / I2C3_SCL / USART3_CTS / OTGHS1_VBUS	-
17	25	33	-	-	-	OTGHS1_R(4)	-	-	OTGHS1 PHY reference current source resistance (12 kΩ ± 1% resistance to digital ground externally)	
18	26	34	-	-	-	OTGHS1_D-(4)	-	-	OTGHS1_D-	
19	27	35	-	-	-	OTGHS1_D+(4)	-	-	OTGHS1_D+	
-	-	-	-	27	35	PB14	I/O	FT	TMR1_CH2N / I2C3_SDA / SPI2_MISO / I2S2_MCK / I2S_SDEXT / USART3_RTS_DE	-
-	-	-	-	28	36	PB15	I/O	FT	RTC_REFIN / TMR1_CH3N / I2C3_SCL / SPI2_MOSI / I2S2_SD	-
20	28	36	-	-	-	V_{DD}	S	-	Digital power supply	
-	-	37	-	-	37	PC6	I/O	FT	TMR1_CH1 / TMR3_CH1 / I2C1_SCL / I2S2_MCK / USART6_TX / UART7_TX	-
-	-	38	-	-	38	PC7	I/O	FT	TMR1_CH2 / TMR3_CH2 / I2C1_SDA / SPI2_SCK / I2S2_CK / I2S3_MCK / USART6_RX / UART7_RX	-
-	-	39	-	-	39	PC8	I/O	FT	TMR1_CH3 / TMR3_CH3 / I2SF5_MCK / UART8_TX / USART6_CK_RTS_DE / QSPI1_IO2	-
-	-	40	-	-	40	PC9	I/O	FT	CLKOUT / TMR1_CH4 / TMR3_CH4 / I2C3_SDA / I2SF5_CKIN / UART8_RX / I2C1_SDA / OTGHS1_OE / QSPI1_IO0	-
-	29	41	18	29	41	PA8	I/O	FT	CLKOUT / TMR1_CH1 / TMR9_BRK / I2C3_SCL / USART1_CK / USART2_TX / UART7_TX / OTGFS1_SOF	-
-	30	42	19	30	42	PA9	I/O	FT	CLKOUT / TMR1_CH2 / I2C3_SMBA / SPI2_SCK / I2S2_CK / USART1_TX / I2C1_SCL / TMR14_BRK / OTGFS1_VBUS	-
-	31	43	20	31	43	PA10	I/O	FT	ERTC_REFIN / TMR1_CH3 / SPI2_MOSI / I2S2_SD / I2SF5_SD / USART1_RX / I2C1_SDA / OTGFS1_ID / I2SF5_MCK	-

Pin number						Pin name (function after reset)	Type (1)	GPIO level(2)	Multiplexed functions (3)	Additional functions
AT32F405			AT32F402							
QFN32	LQFP48/ QFN48	LQFP64	QFN32	LQFP48/ QFN48	LQFP64					
21	32	44	21	32	44	PA11	I/O	FT	TMR1_CH4 / I2C2_SCL / SPI2_CS / I2S2_WS / I2C1_SMBA / USART1_CTS / USART6_TX / CAN1_RX	OTGFS1_D-
22	33	45	22	33	45	PA12	I/O	FT	TMR1_EXT / I2C2_SDA / SPI2_MISO / I2S2_MCK / I2SF5_SDEXT / USART1_RTS_DE / USART6_RX / CAN1_TX	OTGFS1_D+
23	34	46	23	34	46	PA13 (SWDIO(5))	I/O	FT	PA13 / IR_OUT / I2C1_SDA / I2S_SDEXT / SPI3_MISO / I2S3_MCK / OTGFS1_OE	-
-	35	47	-	35	47	PF6	I/O	FT	I2C2_SCL / UART7_RX / QSPI1_IO0	-
-	36	48	-	36	48	PF7	I/O	FT	I2C2_SDA / UART7_TX	-
24	37	49	24	37	49	PA14 (SWCLK(5))	I/O	FT	PA14 / I2C1_SMBA / SPI3_MOSI / I2S3_SD / USART2_TX	-
25	38	50	25	38	50	PA15	I/O	FT	TMR2_CH1 / TMR2_EXT / SPI1_CS / I2S1_WS / SPI3_CS / I2S3_WS / USART1_TX / USART2_RX / UART7_TX / USART4_RTS_DE / QSPI1_IO2	-
-	-	51	-	-	51	PC10	I/O	FT	SPI3_SCK / I2S3_CK / USART3_TX / USART4_TX / QSPI1_IO1	-
-	-	52	-	-	52	PC11	I/O	FT	I2S_SDEXT / SPI3_MISO / I2S3_MCK / USART3_RX / USART4_RX / QSPI1_CS	-
-	-	53	-	-	53	PC12	I/O	FT	TMR11_CH1 / I2C2_SDA / SPI3_MOSI / I2S3_SD / USART3_CK / USART4_CK / USART5_TX	-
-	-	54	-	-	54	PD2	I/O	FT	TMR3_EXT / USART3_RTS_DE / USART5_RX	-
26	39	55	26	39	55	PB3	I/O	FTf	SWO / TMR2_CH2 / I2C2_SDA / SPI1_SCK / I2S1_CK / SPI3_SCK / I2S3_CK / USART1_RX / USART1_RTS_DE / UART7_RX / USART5_TX / QSPI1_IO3	-
27	40	56	27	40	56	PB4	I/O	FT	TMR3_CH1 / TMR11_BRK / I2C3_SDA / SPI1_MISO / I2S1_MCK / SPI3_MISO / I2S3_MCK / USART1_CTS / UART7_TX / USART5_RX / QSPI1_SCK / I2S_SDEXT	-

Pin number						Pin name (function after reset)	Type (1)	GPIO level(2)	Multiplexed functions (3)	Additional functions
AT32F405			AT32F402							
QFN32	LQFP48/ QFN48	LQFP64	QFN32	LQFP48/ QFN48	LQFP64					
28	41	57	28	41	57	PB5	I/O	FT	TMR3_CH2 / TMR10_BRK / I2C3_SMBA / SPI1_MOSI / I2S1_SD / SPI3_MOSI / I2S3_SD / USART1_CK / USART5_RX / USART5_CK_RTS_DE / QSPI1_IO0	WKUP6
29	42	58	29	42	58	PB6	I/O	FT	TMR4_CH1 / TMR10_CH1C / I2C1_SCL / I2S1_MCK / I2SF5_WS / USART1_TX / USART5_TX / USART4_CK / QSPI1_CS	-
30	43	59	30	43	59	PB7	I/O	FT	TMR4_CH2 / TMR11_CH1C / I2C1_SDA / I2SF5_CK / USART1_RX / USART4_CTS / QSPI1_IO1	-
31	44	60	31	44	60	PF11(6) / BOOT0	I/O	FT	-	Boot mode 0
32	45	61	32	45	61	PB8	I/O	FT	TMR2_CH1 / TMR2_EXT / TMR4_CH3 / TMR10_CH1 / I2C1_SCL / I2SF5_SDEXT / USART1_TX / USART5_RX / CAN1_RX / I2SF5_SD	-
-	46	62	-	46	62	PB9	I/O	FTf	IR_OUT / TMR2_CH2 / TMR4_CH4 / TMR11_CH1 / I2C1_SDA / SPI2_CS / I2S2_WS / I2SF5_SD / I2C2_SDA / USART5_TX / CAN1_TX / I2S1_MCK / QSPI1_CS	-
-	47	63	-	47	63	V_{SS}	S	-	Digital ground	
1	48	64	1	48	64	V_{DD}	S	-	Digital power supply	
-	-/49	-	-	-/49	-	EPAD (V_{SS})	S	-	Digital ground	
33	-	-	33	-	-	EPAD (V_{SS} / V_{SSA})	S	-	Digital ground / Analog ground	

(1) I = input, O = output, S = supply.

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog function, FTf = 5 V-tolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull-up resistor. Of those, FTa pin has 5 V-tolerant characteristics when configured as input floating, input pull-up, or input pull-down mode. However, it cannot be 5 V-tolerant in analog mode. In this case, its input level should not be higher than VDD + 0.3 V.

(3) EVENTOUT feature is available on any GPIO.

(4) These are dedicated to OTGHS, not sharing with GPIO or other multiplexed functions.

(5) After reset, PA13/PA14 are configured as multiplexed SWDIO/SWCLK, while the internal pull-up resistor on the SWDIO pin and the internal pull-down resistor of the SWCLK pin are ON.

(6) It is used as BOOT0 during reset, and the boot mode is selected according to its level sampled by the chip. After reset, it is used as PF11 in input pull-down state by default, which can be configured to other states with software.

4 Electrical characteristics

4.1 Test conditions

4.1.1 Minimum and maximum values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

4.1.2 Typical values

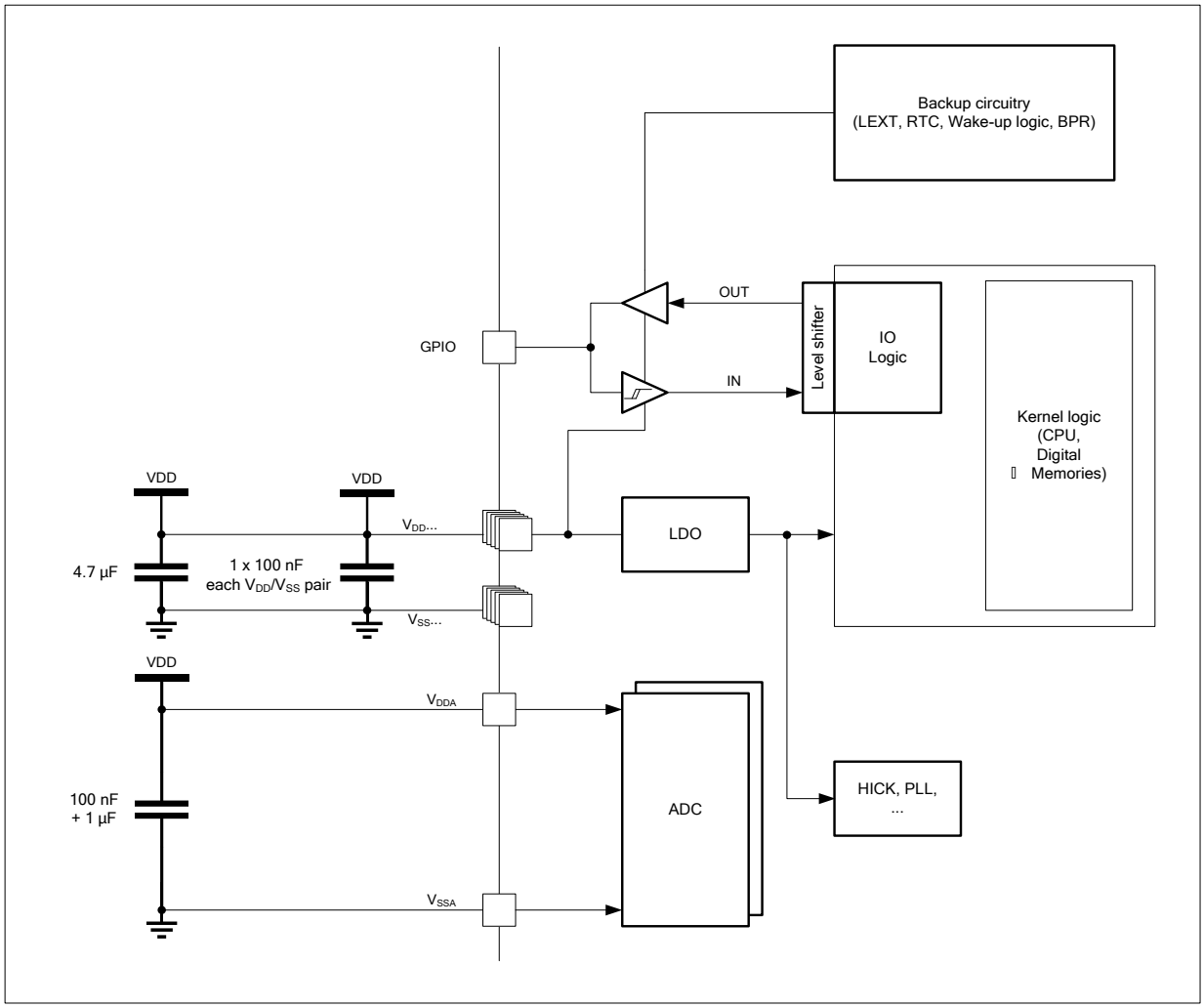
Typical values are based on T_A = 25 °C, V_{DD} = 3.3 V.

4.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

4.1.4 Power supply scheme

Figure 9. Power supply scheme



4.2 Absolute maximum values

4.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 10*,*Table 11* and *Table 12*, it may cause permanent damage to the device. These are the maximum stresses only that the device could withstand, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 10. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DDx}-V_{SS}	External main supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on FT and FTf GPIO	V_{SS}-0.3	6.0	
	Input voltage on FTa GPIO (set as input floating, input pull-up, or input pull-down mode)			
	Input voltage on TC GPIO	V_{SS}-0.3	4.0	
	Input voltage on FTa GPIO (set as analog mode)			
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 11. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	150	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIO and control pin	-25	

Table 12. Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

4.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test is in accordance with the JS-001-2017/JS-002-2018 standard.

Table 13. ESD values

Symbol	Parameter	Conditions	Class	Min	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conform to JS-001-2017	3A	±5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conform to JS-002-2018	III	±1000	

Static latch-up

Tests compliant with EIA/JESD78E IC latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 14. Latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conform to EIA/JESD78E	II level A (±200 mA)

4.3 Specifications

4.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Condition		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	LDO voltage	1.3 V	0	216(1)	MHz
			1.2 V	0	168(1)	
			1.0 V	0	108	
f_{PCLK1}	Internal APB1 clock frequency	LDO voltage	1.3 V, 1.2 V	0	120	MHz
			1.0 V	0	f_{HCLK}	
f_{PCLK2}	Internal APB2 clock frequency	-		0	f_{HCLK}	MHz
V_{DD}	Digital operating voltage	-		2.4	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}		V_{DD}		V
P_D	Power dissipation: T_A = 105 °C	LQFP64 – 10 x 10 mm		-	232	mW
		LQFP64 – 7 x 7 mm		-	212	
		LQFP48 – 7 x 7 mm		-	212	
		QFN48 – 6 x 6 mm		-	350	
		QFN32 – 4 x 4 mm		-	279	
T_A	Ambient temperature	-		-40	105	°C

(1) The maximum allowed frequency of the AHB domain is 120 MHz while accessing CRM_BPDC register and CRM_CTRLSTS register.

4.3.2 Operating conditions at power-up / power-down

Table 16. Operating conditions at power-up/power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	ms/V
	V_{DD} fall time rate	20	∞	μs/V

4.3.3 Embedded reset and power control block characteristics

Table 17. Embedded reset and power control block characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	1.81	2.08	2.4	V
V_{LVR}	Low voltage reset threshold	1.68(2)	1.9	2.08	V
$V_{LVRhyst}$	LVR hysteresis	-	180	-	mV
$T_{RESTTEMPO}$	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RESTTEMPO}$	-	3.5	-	ms

(1) Guaranteed by characterization results, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 10. Power on reset and low voltage reset waveform

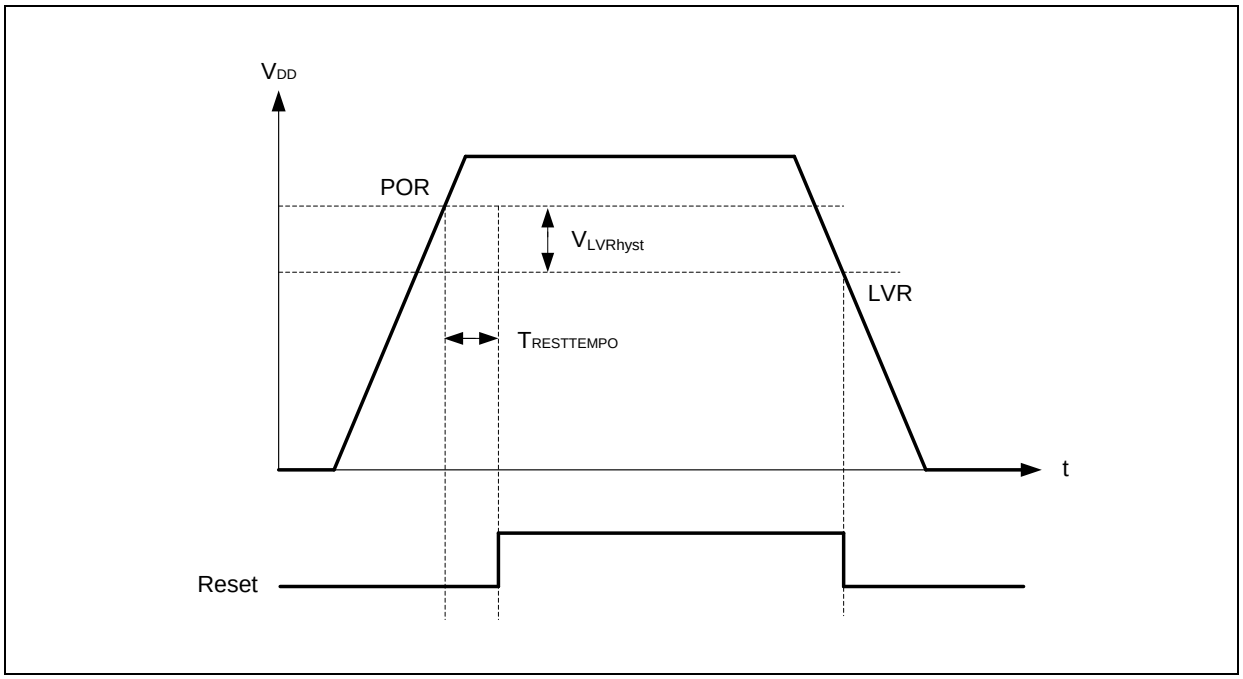


Table 18. Programmable voltage regulator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVM1}	PVM threshold 1 (PVMSEL[2:0] = 001)	Rising edge(1)	2.19	2.28	2.37	V
		Falling edge(1)	2.09	2.18	2.27	V
V_{PVM2}	PVM threshold 2 (PVMSEL[2:0] = 010)	Rising edge(1)	2.28	2.38	2.48	V
		Falling edge(1)	2.18	2.28	2.38	V
V_{PVM3}	PVM threshold 3 (PVMSEL[2:0] = 011)	Rising edge(1)	2.38	2.48	2.58	V
		Falling edge(1)	2.28	2.38	2.48	V
V_{PVM4}	PVM threshold 4 (PVMSEL[2:0] = 100)	Rising edge(1)	2.47	2.58	2.69	V
		Falling edge(1)	2.37	2.48	2.59	V
V_{PVM5}	PVM threshold 5 (PVMSEL[2:0] = 101)	Rising edge(1)	2.57	2.68	2.79	V
		Falling edge(1)	2.47	2.58	2.69	V
V_{PVM6}	PVM threshold 6 (PVMSEL[2:0] = 110)	Rising edge(1)	2.66	2.78	2.9	V
		Falling edge(1)	2.56	2.68	2.8	V
V_{PVM7}	PVM threshold 7 (PVMSEL[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V_{HYS_P}(1)	PVM hysteresis	-	-	100	-	mV
$I_{DD\ (PVM)}$(1)	PVM current dissipation	-	-	18	40	µA

(1) Guaranteed by characterization results, not tested in production.

4.3.4 Memory characteristics

Table 19. Internal Flash memory characteristics (1)

Symbol	Parameter	Condition	Typ	Max	Unit
T_{PROG}	Programming time	-	40	42	μs
t_{SE}	Sector erase time (2 KB)	AT32F405xC/402xC	13.2	16	ms
	Sector erase time (1 KB)	AT32F405xB/402xB	6.6	8	
t_{ME}	Mass erase time	-	8.2	10	ms

(1) Guaranteed by design, not tested in production.

Table 20. Internal Flash memory endurance and data retention (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	year

(1) Guaranteed by design, not tested in production.

4.3.5 Supply current characteristics

The current consumption, obtained by characterization results and not tested in production, is subject to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin toggling rate, and executed binary code.

Typical and maximum current consumption

The device is placed under the following conditions:

- All GPIO pins are in analog mode.
- Flash memory access time depends on the f_{HCLK} frequency (0 ~ 32 MHz : zero-wait state;
- 33 ~ 64 MHz: one wait state; 65 ~ 96 MHz: two wait states; 97 ~ 128 MHz: three wait states; 129 ~ 160 MHz: four wait states, 161 ~ 192 MHz: five wait states, and 193 MHz and above: six wait states)
- Prefetch ON
- When peripherals are enabled:
  - If f_{HCLK} > 120 MHz, then $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/8$
  - If $f_{HCLK} \leq$ 120 MHz, then $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/8$
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition, and the maximum values are measured with V_{DD} = 3.6 V.

Table 21. Typical current consumption in Run mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage (V)	Typ		Unit
					All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1)(2)	216 MHz	1.3	57.1	30.6	mA
			200 MHz	1.3	53.1	28.5	
			180 MHz	1.3	49.8	26.5	
			168 MHz	1.2	40.7	22.0	
			144 MHz	1.2	35.1	19.1	
			120 MHz	1.2	32.7	16.6	
			108 MHz	1.0	24.1	12.2	
			72 MHz	1.0	16.7	8.83	
			48 MHz	1.0	11.7	6.47	
			36 MHz	1.0	9.19	5.21	
			24 MHz	1.0	6.74	4.06	
			12 MHz	1.0	3.59	2.21	
		High speed internal clock (HICK)(2)	216 MHz	1.3	57.0	30.4	mA
			200 MHz	1.3	52.9	28.4	
			180 MHz	1.3	49.6	26.3	
			168 MHz	1.2	40.5	21.8	
			144 MHz	1.2	34.9	18.9	
			120 MHz	1.2	32.5	16.4	
			108 MHz	1.0	23.9	11.9	
			72 MHz	1.0	16.5	8.61	
			48 MHz	1.0	11.5	6.25	
			36 MHz	1.0	8.97	4.99	
			24 MHz	1.0	6.51	3.84	
			12 MHz	1.0	2.56	1.61	

(1) External clock is 12 MHz.
(2) PLL is on when f_{HCLK} > 12 MHz.

Table 22. Typical current consumption in Sleep mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage (V)	Typ		Unit
					All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in sleep mode	High speed external crystal (HEXT)(1)(2)	216 MHz	1.3	43.1	8.92	mA
			200 MHz	1.3	40.0	8.37	
			180 MHz	1.3	36.0	7.75	
			168 MHz	1.2	31.0	7.19	
			144 MHz	1.2	26.8	6.20	
			120 MHz	1.2	25.8	6.23	
			108 MHz	1.0	18.5	4.22	
			72 MHz	1.0	13.2	3.59	
			48 MHz	1.0	9.47	3.03	
			36 MHz	1.0	7.54	2.69	
			24 MHz	1.0	5.72	2.44	
			12 MHz	1.0	3.23	1.52	
		High speed internal clock (HICK)(2)	216 MHz	1.3	42.9	8.64	mA
			200 MHz	1.3	39.8	8.10	
			180 MHz	1.3	35.8	7.51	
			168 MHz	1.2	30.8	6.76	
			144 MHz	1.2	26.6	6.03	
			120 MHz	1.2	25.6	5.80	
			108 MHz	1.0	18.3	3.99	
			72 MHz	1.0	13.0	3.39	
			48 MHz	1.0	9.27	2.83	
			36 MHz	1.0	7.33	2.49	
			24 MHz	1.0	5.50	2.27	
			12 MHz	1.0	2.40	1.26	

(1) External clock is 12 MHz.
(2) PLL is ON when f_{HCLK} > 12 MHz.

Table 23. Maximum current consumption in Run mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage (V)	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1), all peripherals enabled	216 MHz	1.3	67.1	74.3	mA
			200 MHz	1.3	63.1	69.8	
			180 MHz	1.3	59.0	65.1	
			168 MHz	1.2	48.5	54.0	
			144 MHz	1.2	42.8	48.2	
			120 MHz	1.2	40.3	45.7	
			108 MHz	1.0	29.4	33.2	
			72 MHz	1.0	21.4	25.0	
			48 MHz	1.0	16.4	20.0	
			36 MHz	1.0	13.8	17.4	
			24 MHz	1.0	11.4	14.9	
			12 MHz	1.0	8.19	11.7	
		High speed external crystal (HEXT)(1), all peripherals disabled	216 MHz	1.3	39.4	46.0	mA
			200 MHz	1.3	37.4	43.7	
			180 MHz	1.3	35.5	41.2	
			168 MHz	1.2	29.1	34.3	
			144 MHz	1.2	26.2	31.3	
			120 MHz	1.2	23.7	28.8	
			108 MHz	1.0	17.0	20.5	
			72 MHz	1.0	13.3	16.8	
			48 MHz	1.0	11.0	14.5	
			36 MHz	1.0	9.72	13.2	
			24 MHz	1.0	8.55	12.0	
			12 MHz	1.0	6.70	10.1	

(1) External clock is 12 MHz. PLL is ON when f_{HCLK} > 12 MHz.

Table 24. Maximum current consumption in Sleep mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage (V)	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1), all peripherals enabled	216 MHz	1.3	52.7	59.7	mA
			200 MHz	1.3	49.8	56.1	
			180 MHz	1.3	47.1	52.1	
			168 MHz	1.2	38.3	43.7	
			144 MHz	1.2	34.0	39.4	
			120 MHz	1.2	33.0	38.3	
			108 MHz	1.0	23.5	27.5	
			72 MHz	1.0	17.8	21.4	
			48 MHz	1.0	14.0	17.5	
			36 MHz	1.0	12.0	15.5	
			24 MHz	1.0	10.1	13.6	
			12 MHz	1.0	7.58	11.0	
		High speed external crystal (HEXT)(1), all peripherals disabled	216 MHz	1.3	17.1	23.3	mA
			200 MHz	1.3	16.7	22.7	
			180 MHz	1.3	16.3	22.1	
			168 MHz	1.2	13.4	18.3	
			144 MHz	1.2	12.6	17.6	
			120 MHz	1.2	12.4	17.4	
			108 MHz	1.0	8.75	12.1	
			72 MHz	1.0	7.83	11.3	
			48 MHz	1.0	7.25	10.7	
			36 MHz	1.0	6.91	10.3	
			24 MHz	1.0	6.67	10.1	
			12 MHz	1.0	5.73	9.15	

(1) External clock is 12 MHz. PLL is ON when f_{HCLK} > 12 MHz.

Table 25. Typical and maximum current consumptions in Deepsleep and Standby modes

Sym.	Parameter	Condition	Typ(1)		Max(2)			Unit
			V_{DD} = 2.4 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode (3)	LDO in Run mode, HICK and HEXT OFF, WDT OFF	895	900	See(4)	7600	12600	µA
		LDO in low-power mode, LPDS1=1, HICK and HEXT OFF, WDT OFF	463	465		4200	7300	
	Supply current in Standby mode	LEXT and ERTC OFF	2.4	3.7	4.7	6.1	8.6	µA
		LEXT and ERTC ON	3.4	5.1	6.3	7.8	10.3	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.
(3) OTGHS must be configured in low-power mode before the entry of Deepsleep mode. Refer to AT32F405/402 errata sheet for details.
(4) This value may be several times the typical one due to process variations.

Figure 11. Typical current consumption in Deepsleep mode with LDO in run mode vs. temperature at different V_{DD}

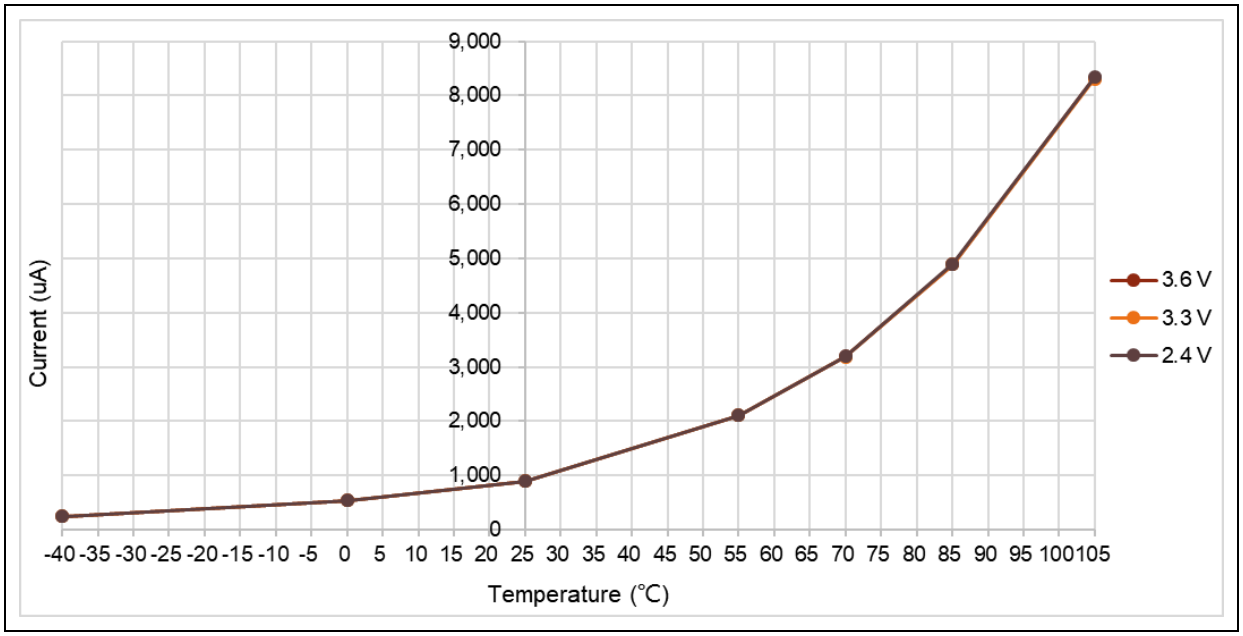


Figure 12. Typical current consumption in Deepsleep mode with LDO in low-power mode vs. temperature at different V_{DD}

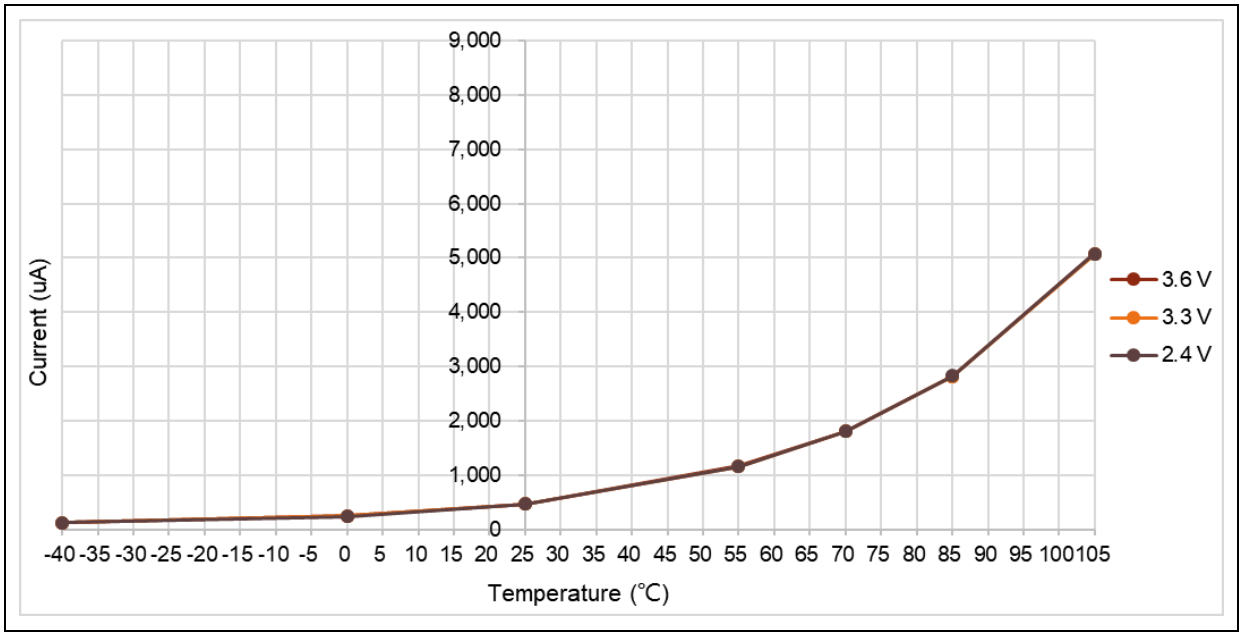
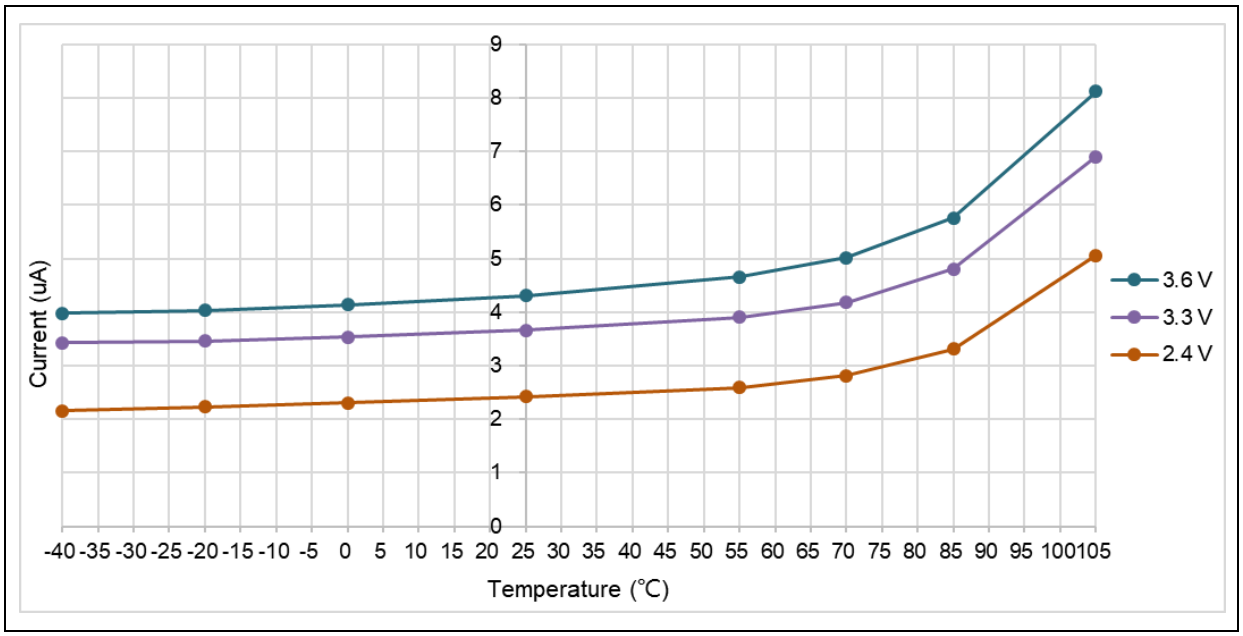


Figure 13. Typical current consumption in Standby mode vs. temperature at different V_{DD}



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 26. Peripheral current consumption

Peripheral		LDO voltage (V)			Unit
		1.3	1.2	1.0	
AHB	DMA1	4.11	3.78	3.00	μA/MHz
	DMA2	4.07	3.73	2.99	
	SRAM	1.42	1.32	1.09	
	Flash	16.39	14.77	11.85	
	CRC	0.38	0.36	0.31	
	GPIOA	0.45	0.44	0.37	
	GPIOB	0.45	0.43	0.35	
	GPIOC	0.45	0.44	0.35	
	GPIOD	0.46	0.44	0.35	
	GPIOF	0.45	0.44	0.35	
	OTGHS1	18.42	16.58	13.53	
	OTGFS1	15.89	14.35	11.96	
	QSPI1	14.13	12.65	10.17	
APB1	TMR2	8.61	7.80	7.32	μA/MHz
	TMR3	6.44	5.84	5.25	
	TMR4	7.31	6.63	6.00	
	TMR6	0.37	0.37	0.36	
	TMR7	0.37	0.36	0.34	
	TMR13	3.24	2.95	2.74	
	TMR14	3.30	2.99	2.71	
	WWDT	0.11	0.09	0.08	
	SPI2/I^2S2	2.42	2.24	1.79	
	SPI3/I^2S3	2.47	2.27	1.81	
	USART2	2.66	2.42	1.98	
	USART3	2.63	2.42	1.98	
	USART4	2.75	2.49	1.99	
	USART5	2.65	2.42	1.98	
	I^2C1	6.28	5.57	4.38	
	I^2C2	6.37	5.68	4.68	
	I^2C3	6.31	5.66	4.41	
	CAN1	2.62	2.44	1.96	
	PWC	0.43	0.39	0.33	
	UART7	2.66	2.44	1.98	
	UART8	2.67	2.42	1.94	

Peripheral		LDO voltage (V)			Unit
		1.3	1.2	1.0	
APB2	TMR1	10.18	9.24	7.53	μA/MHz
	USART1	2.59	2.36	1.93	
	USART6	2.63	2.40	1.95	
	ADC1	2.07	1.90	1.55	
	SPI1/I^2S1	2.53	2.32	1.91	
	SCFG	0.09	0.08	0.07	
	TMR9	5.92	5.34	4.34	
	TMR10	3.63	3.29	2.69	
	TMR11	3.74	3.39	2.77	
	I^2SF5	1.00	0.95	0.77	
	ACC	0.23	0.20	0.17	

4.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be generated with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

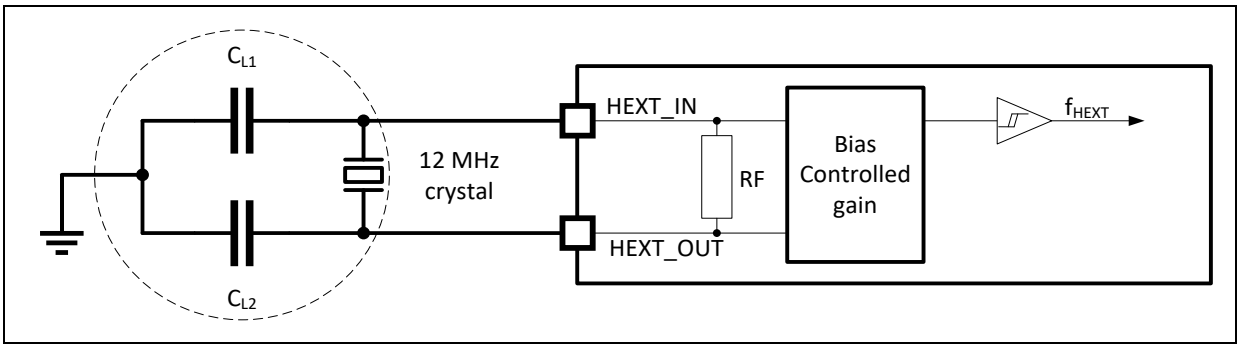
Table 27. HEXT 4 ~ 25 MHz crystal characteristics (1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HEXT_IN}	Oscillator frequency	-	4	12	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	V_{DD} is stabilized	-	1.6	-	ms

(1) Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 12 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be taken into account (10 pF can be used as a rough estimate of the combined pin and board capacitance) when selecting C_{L1} and C_{L2}.

Figure 14. HEXT typical application with 12 MHz crystal



High-speed external clock generated from an external source

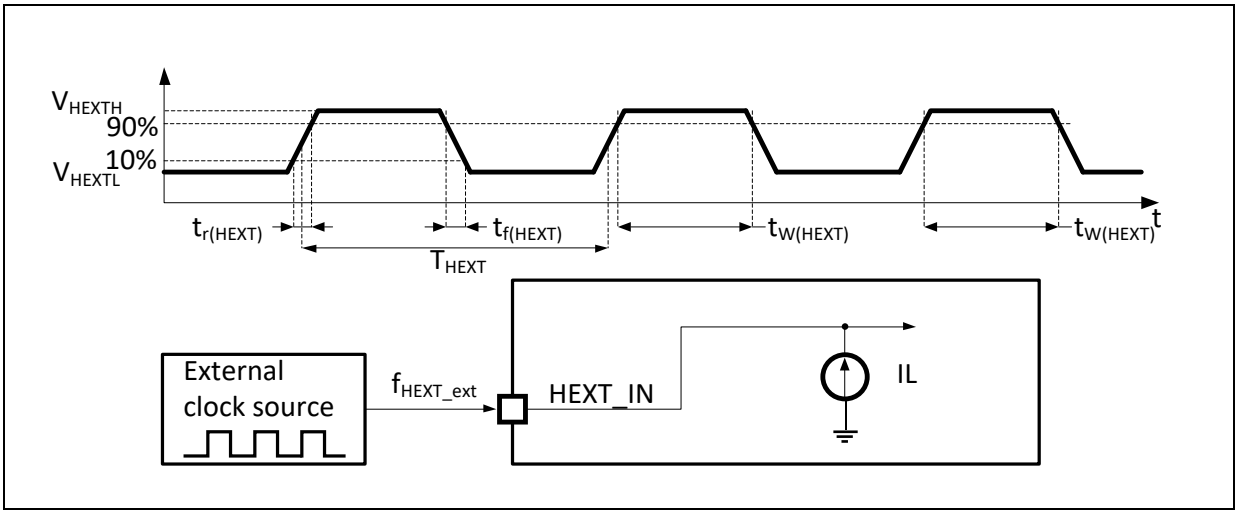
The characteristics given in the table below come from tests performed using a high-speed external clock source.

Table 28. HEXT external source characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency (1)	-	1	12	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time (1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time (1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance (1)	-	-	5	-	pF
$Duty_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be generated with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. LEXT 32.768 kHz crystal characteristics (1)(2)

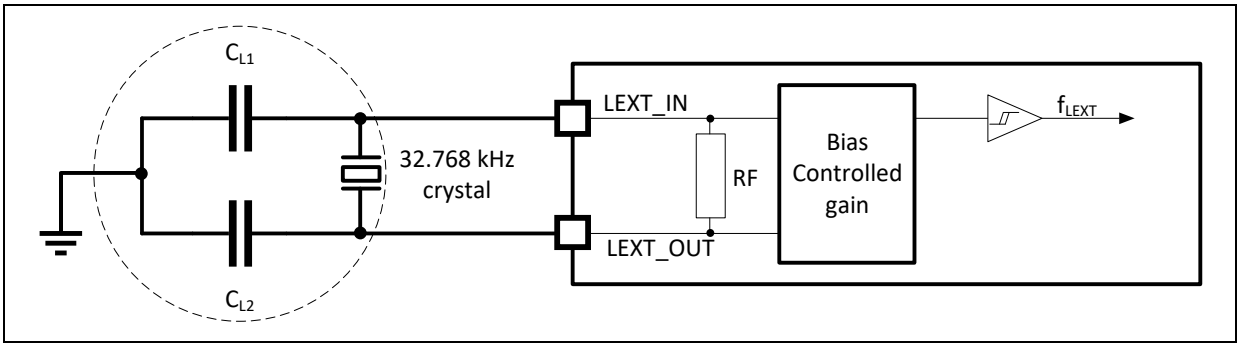
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	V_{DD} is stabilized	-	160	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range and select to meet the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 16. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.

Low-speed external clock generated from an external source

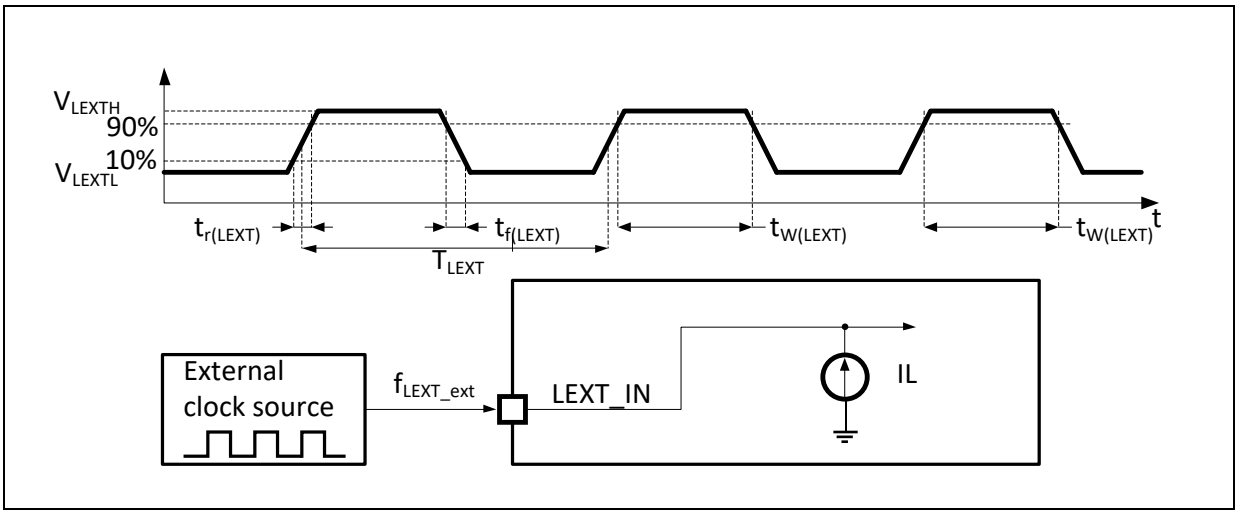
The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 30. Low-speed external source characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LEXT_ext}	User external clock source frequency (1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time (1)		450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time (1)		-	-	50	
$C_{in(LEXT)}$	LEXT_IN input capacitance (1)	-	-	5	-	pF
$Duty_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 17. Low-speed external clock source AC timing diagram



4.3.7 Internal clock source characteristics

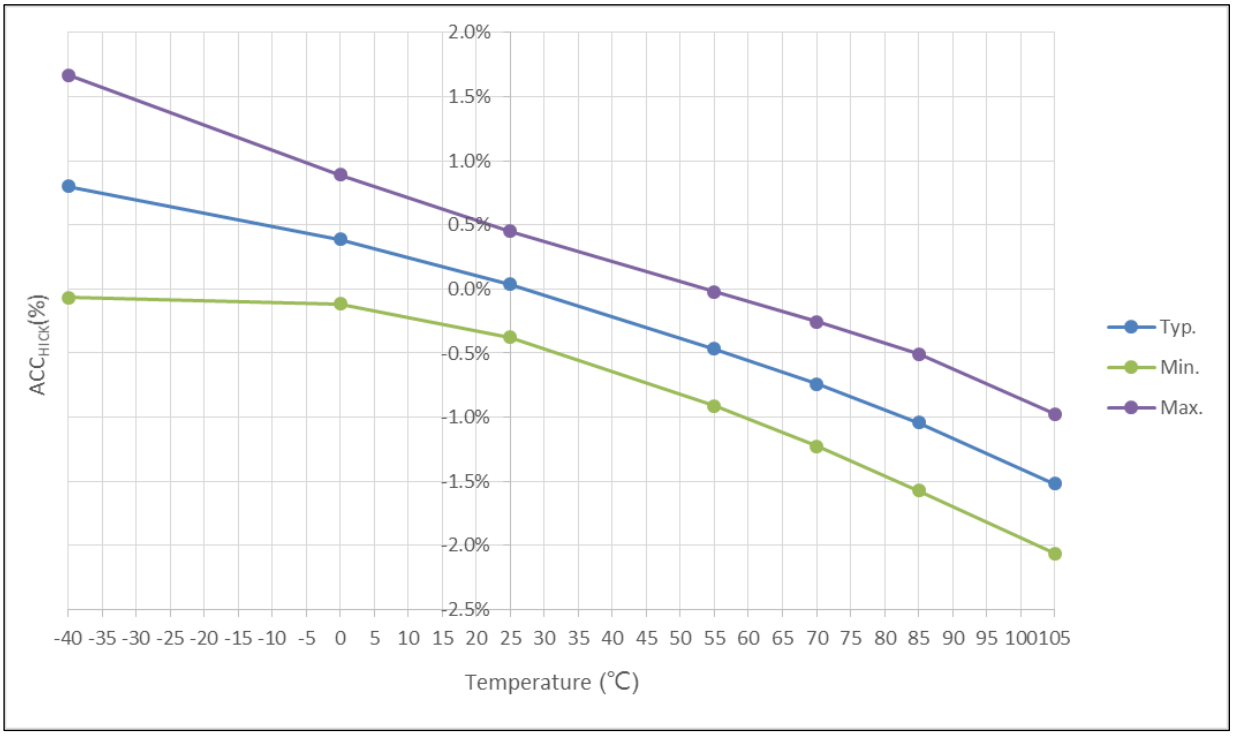
High-speed internal clock (HICK)

Table 31. HICK clock characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	Accuracy of the HICK oscillator	User-trimmed with the CRM_CTRL register (1)		-1	-	1	%
		ACC-trimmed (1)		-0.25	-	0.25	
		Factory-calibrated (2)	T_A = -40 ~ 105 °C	-2.5	-	2.5	
			T_A = -40 ~ 85 °C	-2	-	2	
			T_A = 0 ~ 70 °C	-1.5	-	1.5	
			T_A = 25 °C	-1	0.5	1	
$t_{SU(HICK)}$(2)	HICK oscillator startup time	-		-	2.0	2.4	µs
$I_{DD(HICK)}$(2)	HICK oscillator power consumption	-		-	315	370	µA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 18. HICK clock frequency accuracy vs. temperature



Low-speed internal clock (LICK)

Table 32. LICK clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	25	35	45	kHz

(1) Guaranteed by characterization results, not tested in production.

4.3.8 PLL characteristics

Table 33. PLL characteristics

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	12	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	216	MHz
t_{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Use the appropriate multiplier factor to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

4.3.9 Wakeup time from low-power mode

The wakeup times given in the table below are measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: The clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: The clock source is the HICK.

Table 34. Low-power mode wakeup time

Symbol	Parameter	Condition	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	3.4	μs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode	LDO in Run mode	450	μs
		LDO in low-power mode	500	
$t_{WUSTDBY}$	Wakeup from Standby mode	-	800	μs

4.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional error occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 35. EMS characteristics

Sym.	Parameter	Condition	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforming to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional error. Both V_{DD} and V_{SS} have a 47 µF capacitor on their entries. Each V_{DD} and V_{SS} pair has 0.1 µF bypass capacitor.	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 216 MHz, LDO 1.3 V	4A (±4 kV)
		V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 168 MHz, LDO 1.2 V	
		V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 108 MHz, LDO 1.0 V	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC optimization and prequalification tests in relation with the EMC level.

4.3.11 GPIO port characteristics

General input/output characteristics

All GPIOs are CMOS and TTL compliant.

Table 36. GPIO static characteristics

Sym.	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	-0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	TC GPIO input high level voltage	-	0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FTa GPIO input high level voltage	Analog mode				
	FT and FTf GPIO input high level voltage	-		-	5.5	
	FTa GPIO input high level voltage	Input floating, input pull-up, or input pull-down mode				
V_{hys}	Schmitt trigger voltage hysteresis (1)	-	200	-	-	mV
			5% V_{DD}	-	-	-
I_{lkg}	Input leakage current (2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC GPIOs	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5$ V FT, FTf and FTa GPIOs	-	-	±1	
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	65	80	130	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)(4)	$V_{IN} = V_{DD}$	65	70	130	kΩ
C_{IO}	GPIO pin capacitance	-	-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels.Guaranteed by characterization results, not tested in production.
(2) Leakage could be higher than the max if negative current is injected on adjacent pins.
(3) When the input is higher than V_{DD} + 0.3 V, the internal pull-up and pull-down resistors must be disabled for FT, FTf and FTa pins.
(4) The weak pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins that can drive current must be controlled to respect the absolute maximum rating defined in *Section 4.2.1*.

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 11*).
- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 11*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 37. Output voltage characteristics (1)

Symbol	Parameter	Condition	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL port, I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}	Output low level voltage	I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL port, I_{IO} = 5 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}	Output low level voltage	I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Maximum sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 15 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL port, I_{IO} = 12 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 12 mA	-	0.4	V
V_{OH}	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Ultra high sinking strength (2)					
V_{OL}	Output low level voltage	I_{IO} = 25 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OL}	Output low level voltage	I_{IO} = 18 mA, 2.4 V ≤ V_{DD} < 2.7 V			

(1) Guaranteed by characterization results, not tested in production.
(2) When GPIO ultra high sinking strength is enabled, its V_{OH} is the same as that of maximum sourcing strength.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 38. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$(1)	Pulse width of external signals detected by EXINT controller	10	-	ns

(1) Guaranteed by design, not tested in production.

4.3.12 NRST pin characteristics

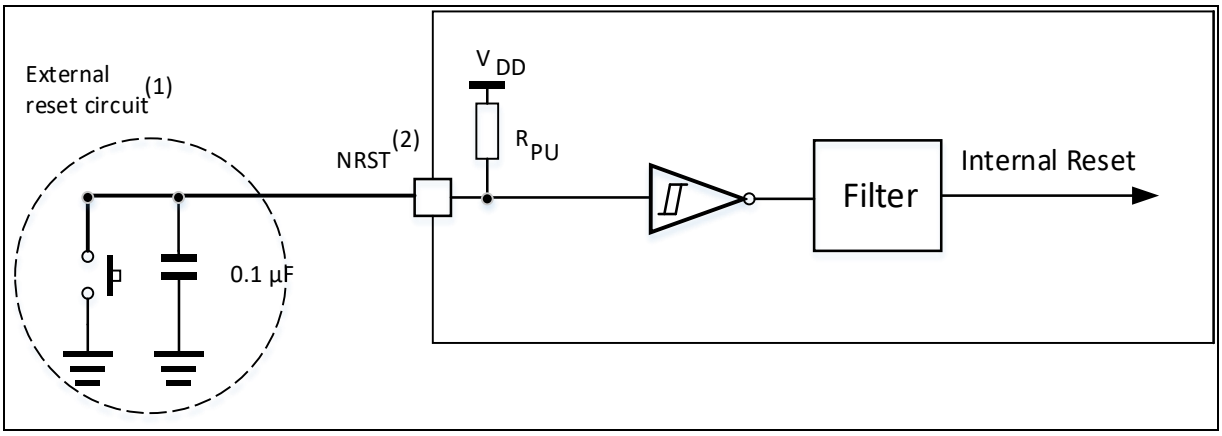
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 39. NRST pin characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.3	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	500	-	mV
R_{PU}(2)	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	30	40	50	kΩ
$t_{ILV(NRST)}$(1)	NRST input low level inactive	-	-	-	40	μs
$t_{ILNV(NRST)}$(1)	NRST input low level active	-	80	-	-	μs

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 19. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the $V_{IL\ (NRST)}$ max level specified in *Table 39*. Otherwise, the reset will not be performed by the device.

4.3.13 TMR timer characteristics

The parameters given in the table below are guaranteed by design and not tested in production.

Table 40. TMR timer characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 216 MHz	4.63	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz

4.3.14 SPI characteristics

Table 41. SPI characteristics

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})^{(1)}$	SPI clock frequency (2)(3)	Master mode	-	36	MHz
		Slave receive mode	-	36	
		Slave transmit mode	-	25	
$t_{su(CS)}^{(1)}$	CS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(CS)}^{(1)}$	CS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode Prescaler factor = 4	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{su(MI)}^{(1)}$	Data input setup time	Master mode	6	-	ns
$t_{su(SI)}^{(1)}$		Slave mode	5	-	
$t_{h(MI)}^{(1)}$	Data input hold time	Master mode	4	-	ns
$t_{h(SI)}^{(1)}$		Slave mode	5	-	
$t_{a(SO)}^{(1)(4)}$	Data output acess time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{dis(SO)}^{(1)(5)}$	Data output disable time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enable edge)	-	10	ns
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	9	-	ns
$t_{h(MO)}^{(1)}$		Master mode (after enable edge)	2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales representative.
(4) Min time is the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 20. SPI timing diagram – slave mode and CPHA = 0

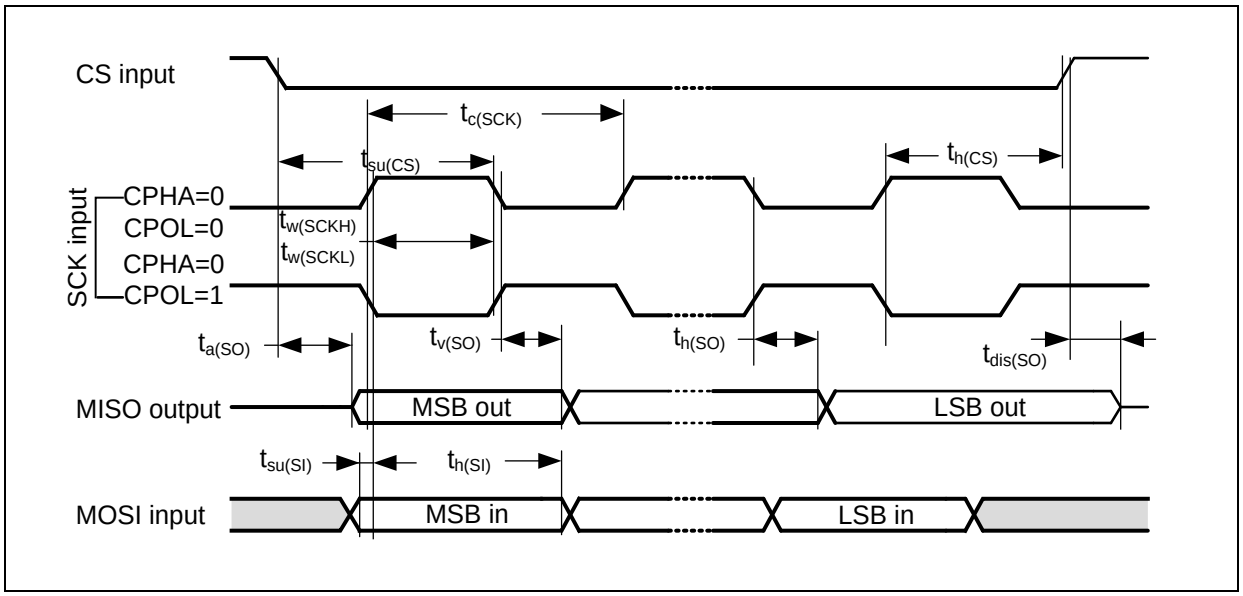


Figure 21. SPI timing – slave mode and CPHA = 1

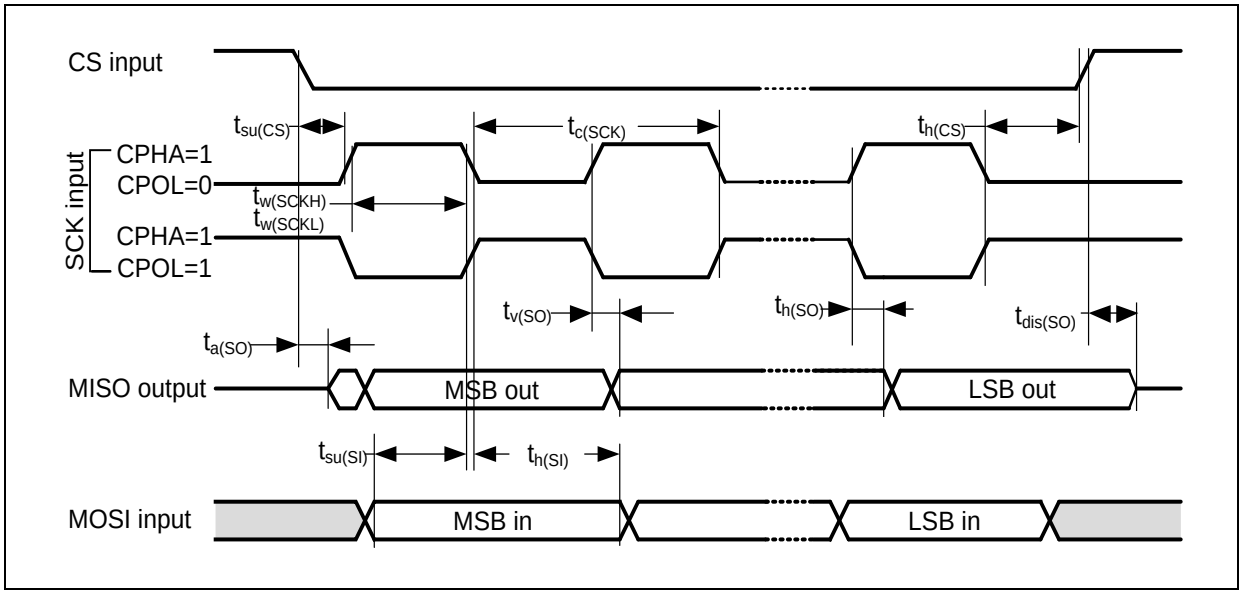
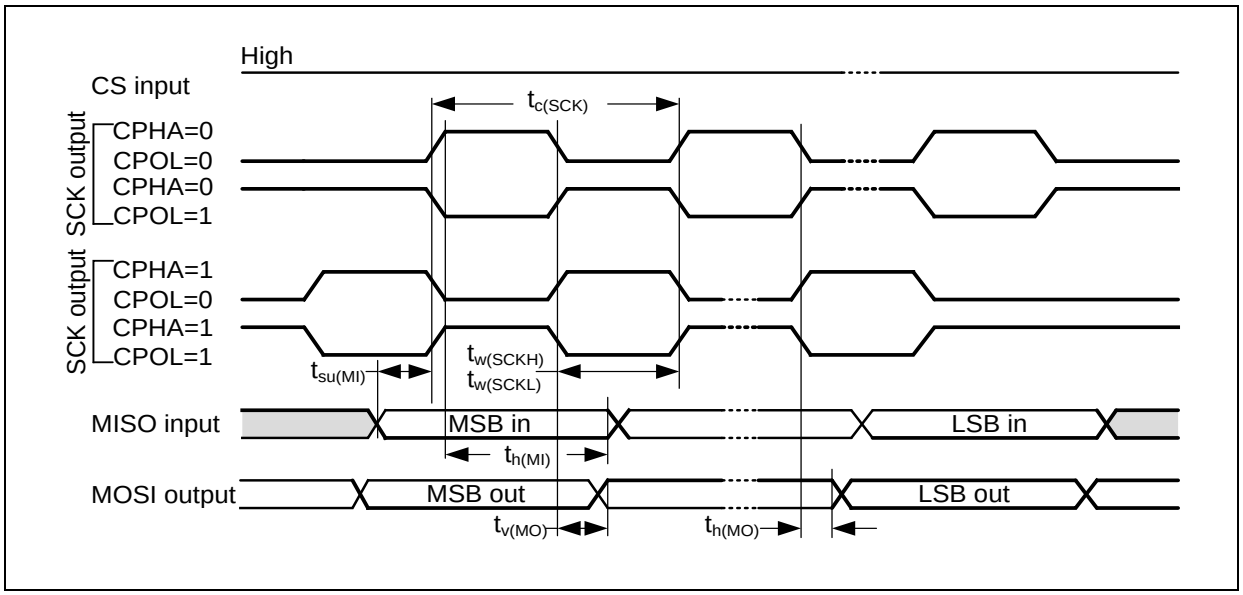


Figure 22. SPI timing – master mode



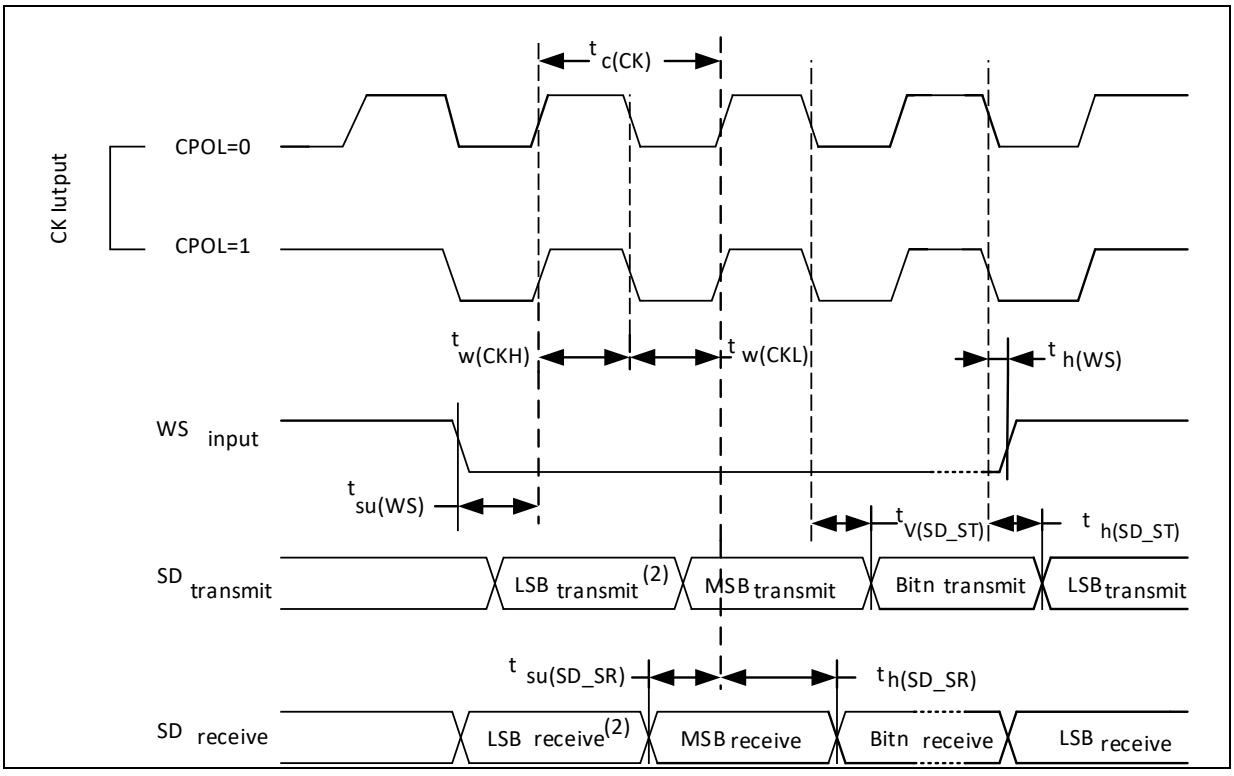
4.3.15 I²S / I²SF characteristics

Table 42. I²S/I²SF characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 15 pF	-	12	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	0	4	
$t_{h(WS)}$(1)	WS hold time	Master mode	0	4	
$t_{su(WS)}$(1)	WS setup time	Slave mode	9	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	2	-	
$t_{h(SD\_MR)}$(1)	Data input hold time	Master receiver	0.5	-	
$t_{h(SD\_SR)}$(1)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_MT)}$(1)	Data output valid time	Master transmitter (after enable edge)	-	15	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

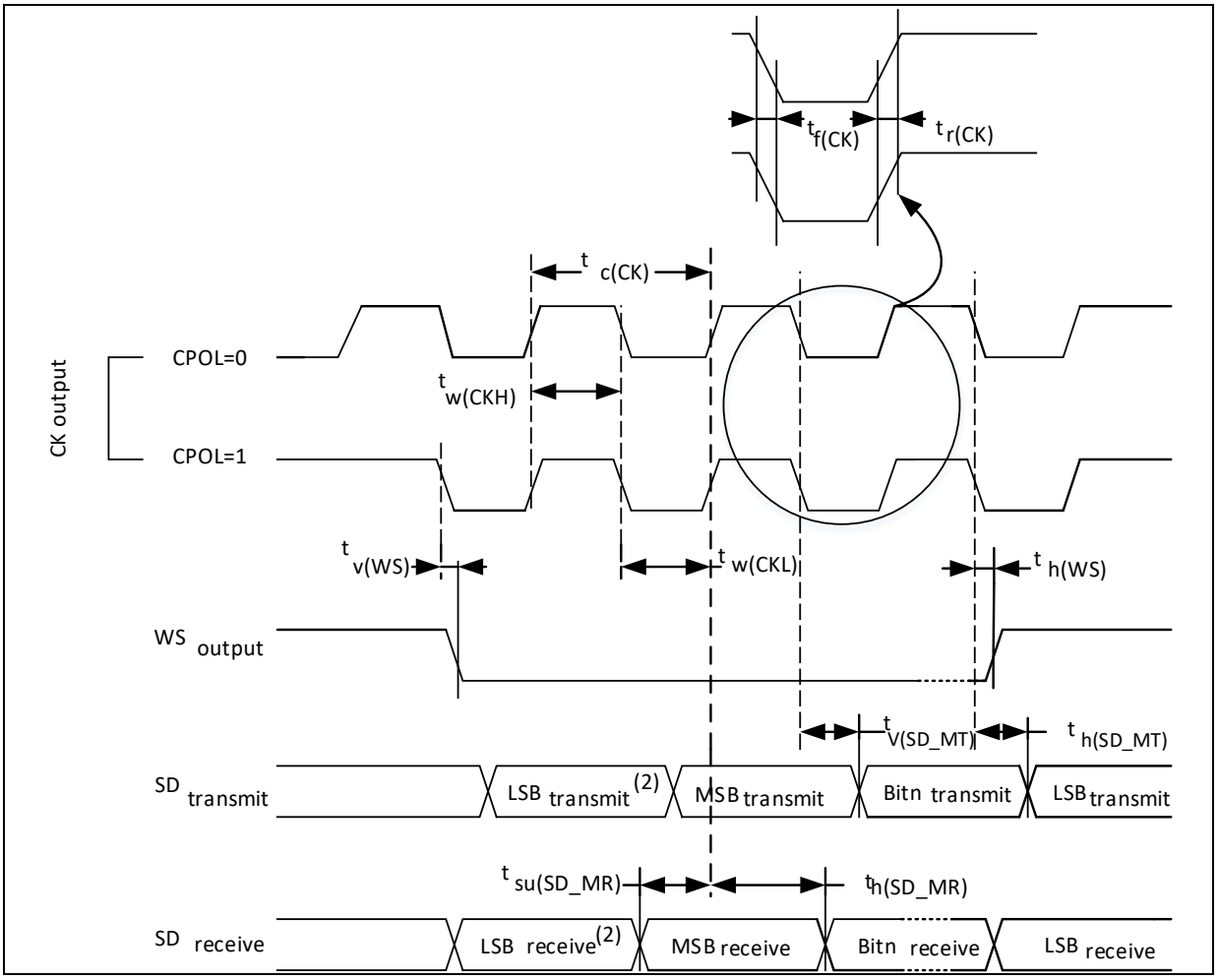
(1) Guaranteed by design, not tested in production.

Figure 23. I²S/I²SF slave timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 24. I²S/I²SF master timing diagram (Philips protocol)



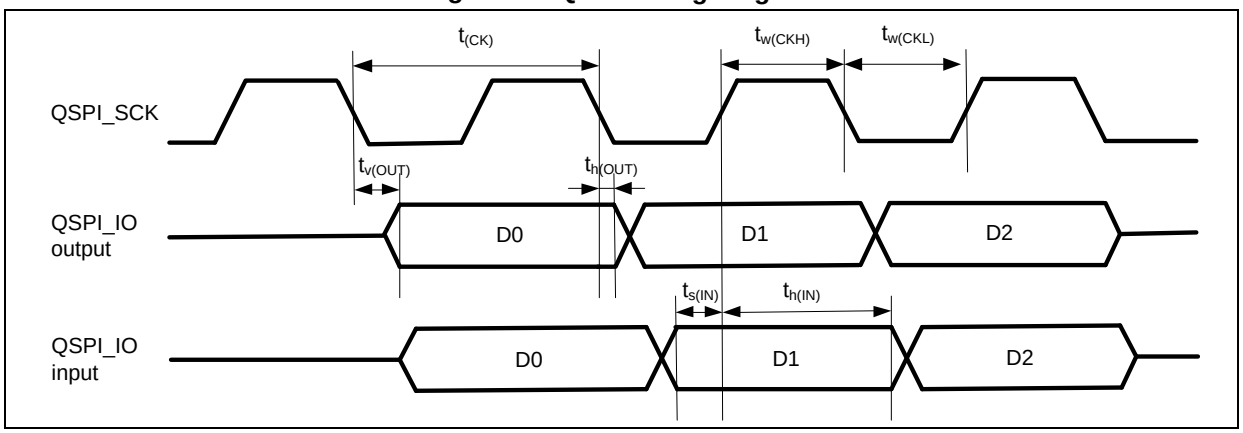
(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

4.3.16 QSPI characteristics

Table 43. QSPI characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCK} $1/t_{(CK)}$	QSPI clock frequency	-	-	-	108	MHz
$t_{w(CKH)}$	QSPI clock high and low time	-	$(t_{(CK)} / 2) - 2$	-	$t_{(CK)} / 2$	ns
$t_{w(CKL)}$			$t_{(CK)} / 2$	-	$(t_{(CK)} / 2) + 2$	ns
$t_{s(IN)}$	Data input setup time	-	2	-	-	ns
$t_{h(IN)}$	Data input hold time	-	4.5	-	-	ns
$t_{v(OUT)}$	Data output valid time	-	-	1.5	3	ns
$t_{h(OUT)}$	Data output hold time	-	0	-	-	ns

Figure 25. QSPI timing diagram



4.3.17 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not “true” open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz).

4.3.18 OTGHS characteristics

Table 44. OTGHS DC electrical characteristics

Symbol		Parameter	Condition	Min(1)	Typ	Max(1)	Unit
V_{DD}		OTGHS operating voltage	-	3.0	-	3.6	V
Input levels	V_{DI}(2)	Differential input sensitivity	I (OTGHS_D+/D-)	300	-	-	mV
	V_{CM}(2)	Differential common mode range	-	-50	-	500	
	V_{SQ}(2)	Squelch detection threshold	-	100	-	200	
	V_{DSC}(2)	Disconnection detection threshold	-	525	-	625	
Output levels (differential)	V_{OI}	Idle output	-	-20	-	20	mV
	V_{OL}	Low level output	-	-20	-	20	
	V_{OH}	High level output	-	360	400	440	
	V_{CHIRPJ}	Chirp J output	-	700	-	1100	
	V_{CHIRPK}	Chirp K output	-	-900	-	-500	
R_{REF}		OTGHS_R external resistance	-	11.88	12	12.12	kΩ
I_{DD}		Supply current in RUN mode (current consumption difference between data transfer and non-data transfer)	f_{HCLK} = 168 MHz, LDO = 1.2 V	-	25.9	-	mA

(1) All the voltages are measured from the local ground potential.
(2) Guaranteed by design, not tested in production.

Table 45. OTGHS DC electrical characteristics

Symbol	Parameter	Condition	Min(1)	Typ	Max(1)	Unit
t_r	Rise time (2)	-	100	-	-	ps
t_f	Fall time (2)	-	100	-	-	ps
Z_{DRV}	Output driver impedance	-	40.5	45	49.5	Ω

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal.

4.3.19 OTGFS characteristics

Table 46. OTGFS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	OTGFS transceiver startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 47. OTGFS DC electrical characteristics

Symbol		Parameter	Condition	Min(1)	Typ	Max(1)	Unit
V_{DD}		OTGFS operating voltage	-	3.0(2)	-	3.6	V
Input levels	V_{DI}(3)	Differential input sensitivity	I (OTGFS_D+/D-)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Include V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	1.24 kΩ R_L to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	15 kΩ R_L to V_{SS}(4)	2.8	-	3.6	
R_{PU}		OTGFS_D+ internal pull-up	V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ
R_{PD}		OTGFS_D+/D- internal pull-down	V_{IN} = V_{DD}	15	19	25	kΩ

(1) All the voltages are measured from the local ground potential.
(2) The AT32F405/402 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics that are degraded in the 2.7 to 3.0 V V_{DD} voltage range.
(3) Guaranteed by design, not tested in production.
(4) R_L is the load connected to the USB drivers.

Figure 26. OTGFS timings: definition of data signal rise and fall time

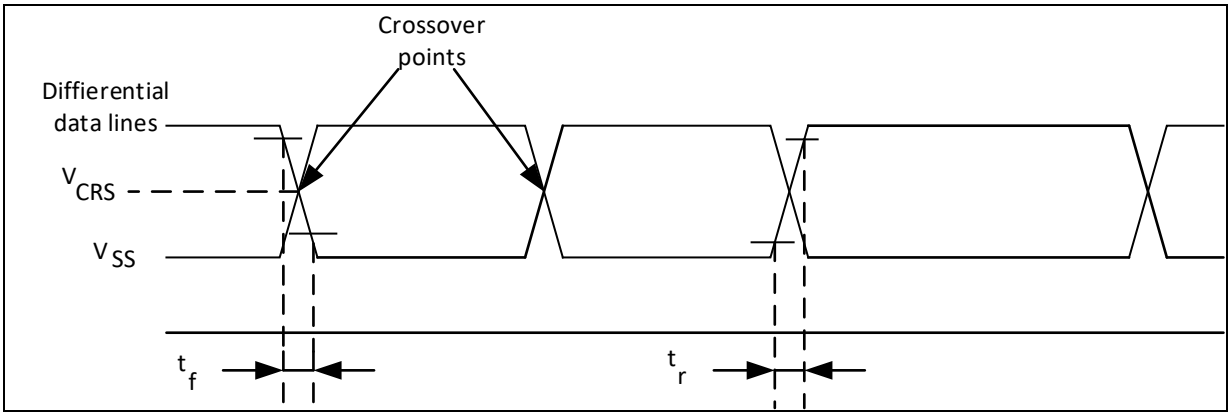


Table 48. OTGFS electrical characteristics

Symbol	Parameter	Condition	Min(1)	Max(1)	Unit
t_r	Rise time (2)	$C_L \leq 50$ pF	4	20	ns
t_f	Fall time (2)	$C_L \leq 50$ pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification Chapter 7 (version 2.0).

4.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 15*.

Note: It is recommended to perform a calibration after each power-up.

Table 49. ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	475(1)	560	μA
f_{ADC}	ADC clock frequency	-	0.6	-	28	MHz
f_S(2)	Sampling rate	-	0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range (3)	-	0 (V_{REF-} connected to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table 50* and *Table 51*			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	8.5	13	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	6.61			μs
		-	185			$1/f_{ADC}$
t_{latr}(2)	Trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	ns
		-	-	-	2(4)	$1/f_{ADC}$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	1/f_{ADC}
t_{STAB}(2)	Power-up time	-	42			1/f_{ADC}
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	μs
		-	14~252 (t_S or sampling + 12.5 for successive approximation)			1/f_{ADC}

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} may be connected to V_{DDA} internally, and V_{REF-} to V_{SSA}.
(4) For external triggers, a delay of 1/f_{PCLK2} must be added to the latency.

Table 50 and *Table 51* define the maximum external impedance allowed for an error below 1 LSB.

Table 50. R_{AIN} max when f_{ADC} = 14 MHz (1)

T_S (cycle)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.11	0.35
7.5	0.54	3.9
13.5	0.96	7.4
28.5	2.04	16.3
41.5	2.96	24.0
55.5	3.96	32.3
71.5	5.11	41.8
239.5	17.11	50.0

(1) Guaranteed by design.

Table 51. R_{AIN} max when f_{ADC} = 28 MHz (1)

T_S (cycle)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.05	0.1
7.5	0.27	1.6
13.5	0.48	3.4
28.5	1.02	7.9
41.5	1.48	11.7
55.5	1.98	15.9
71.5	2.55	20.6
239.5	8.55	50.0

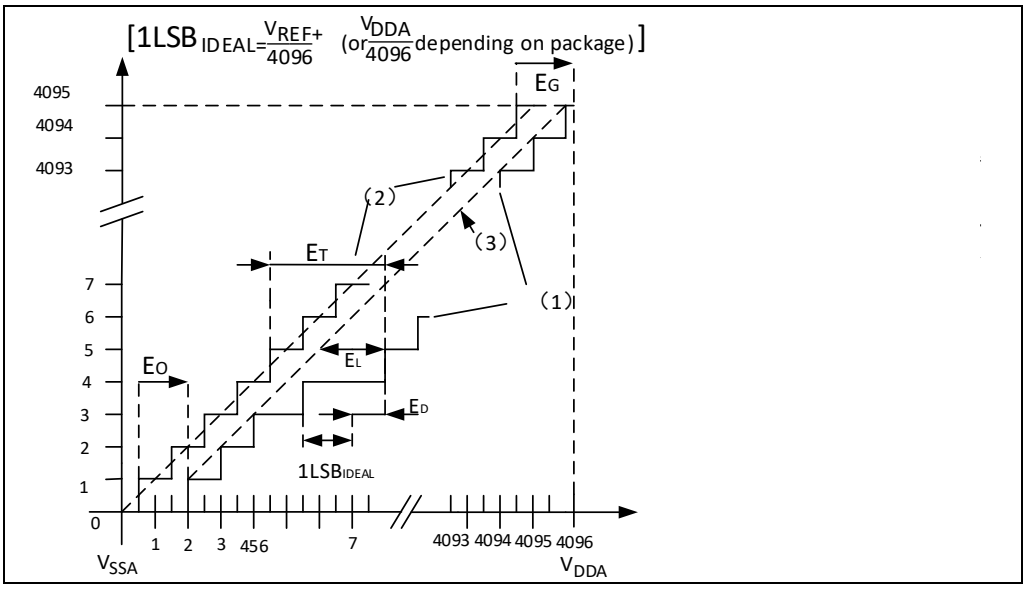
(1) Guaranteed by design.

Table 52. ADC accuracy (1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0~3.6 V, T_A = 25 °C	±2	±3	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±1.5	±2.5	
ED	Differential linearity error		±0.8	±1	
EL	Integral linearity error		±1.2	±1.5	
ET	Total unadjusted error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4~3.6 V, T_A = -40 ~ 105 °C	±3	±4	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±2	±3	
ED	Differential linearity error		±1	-1/+1.5	
EL	Integral linearity error		±1.5	±2.5	

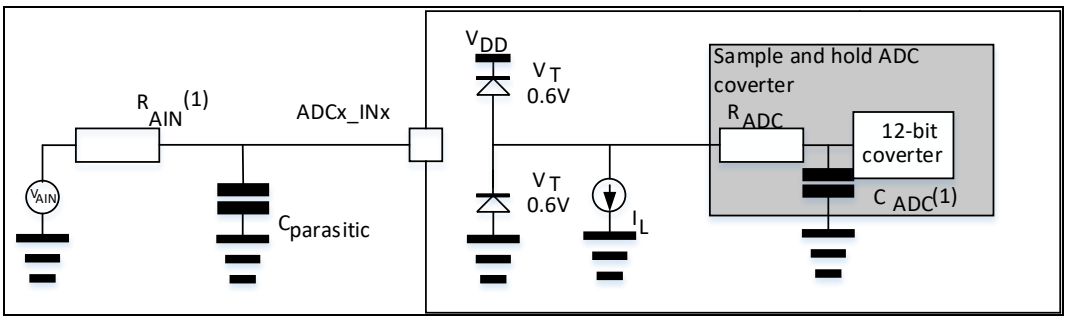
(1) ADC DC accuracy values are measured after internal calibration.
(2) Guaranteed by characterization results, not tested in production.

Figure 27. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
E_T = Maximum deviation between the actual and the ideal transfer curves.
E_O = Deviation between the first actual transition and the first ideal one.
E_G = Deviation between the last ideal transition and the last actual one.
E_D = Maximum deviation between actual steps and the ideal one.
E_L = Maximum deviation between any actual transition and the end point correlation line.

Figure 28. Typical connection diagram using the ADC



(1) Refer to *Table 49* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9*. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

4.3.21 Internal reference voltage (V_{INTRV}) characteristics

Table 53. Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	-	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature coefficient	-	-	50	100	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading the internal reference voltage	-	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

4.3.22 Temperature sensor (V_{TS}) characteristics

Table 54. Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	T_A = -10 ~ +70 °C	-	±1	±2	ºC
		T_A = -40 ~ +105 °C	-	-	±3.5	
Avg_Slope(1)(2)	Average slope	-	--1.59	-1.69	-1.79	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	-	460	490	520	mV
t_{START}(3)	Startup time	-	-	-	20	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	-	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 20 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

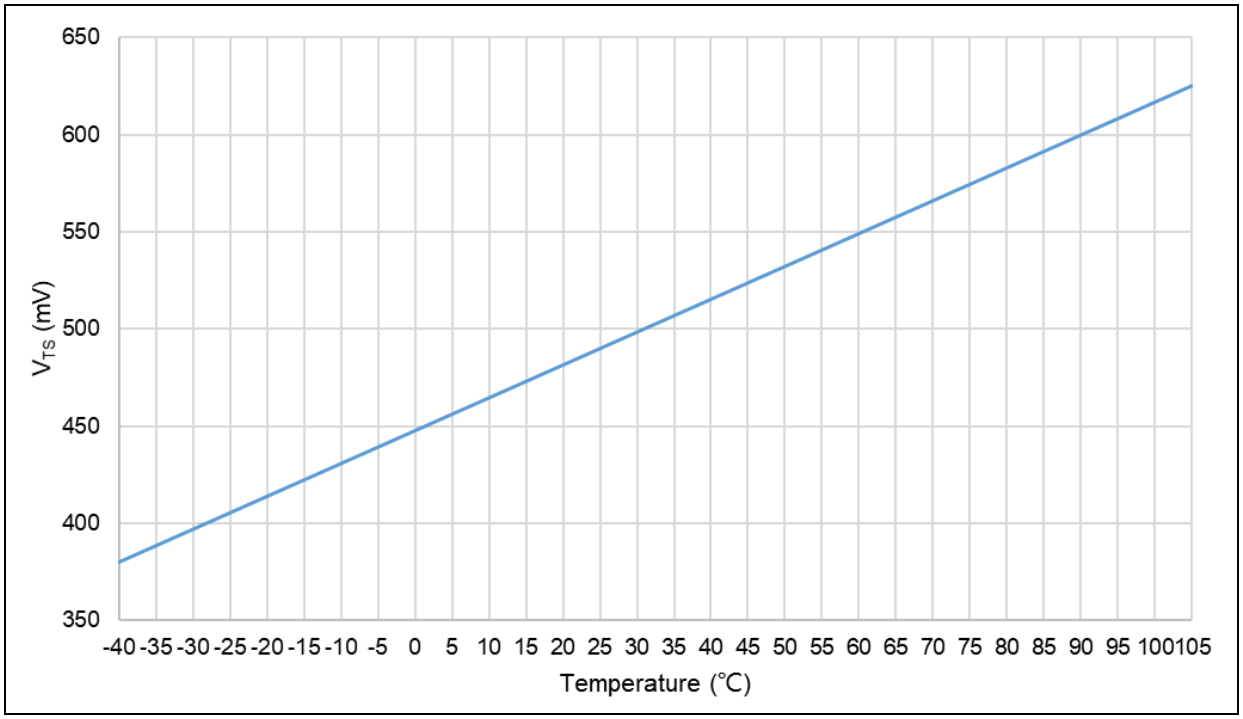
Temperature (°C) = {(V_{25} – V_{TS}) / Avg_Slope} + 25

Where,

V_{25} = V_{TS} value for 25 °C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{TS} (given in mV/°C)

Figure 29. V_{TS} vs. temperature



5 Package information

5.1 LQFP64 – 10 x 10 mm

Figure 30. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline

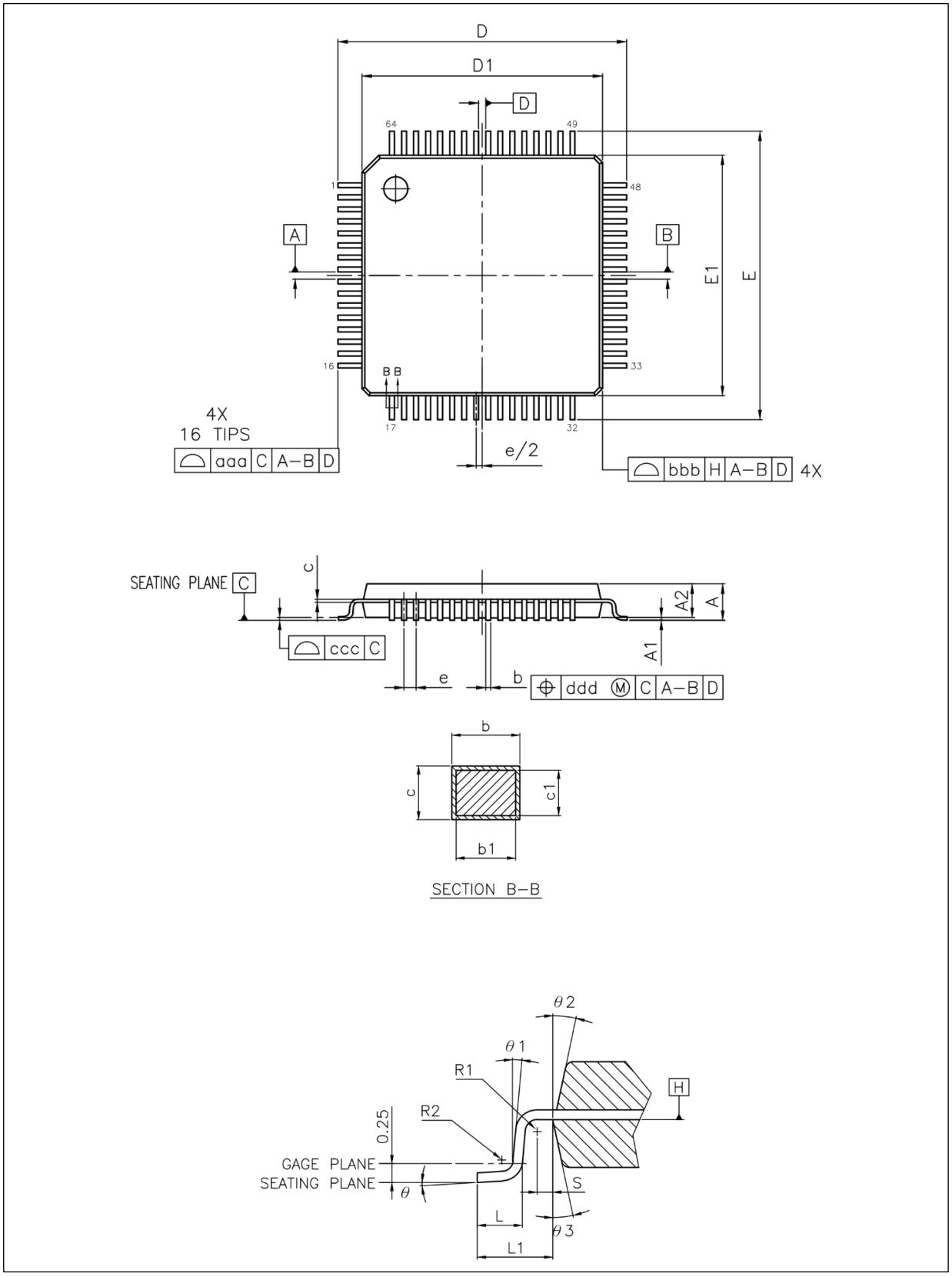


Table 55. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	-	0.20
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC.		
Θ	3.5° REF.		
L	0.45	0.60	0.75
L1	1.00 REF.		
ccc	0.08		

5.2 LQFP64 – 7 x 7 mm

Figure 31. LQFP64 – 7 x 7 mm 64 pin low-profile quad flat package outline

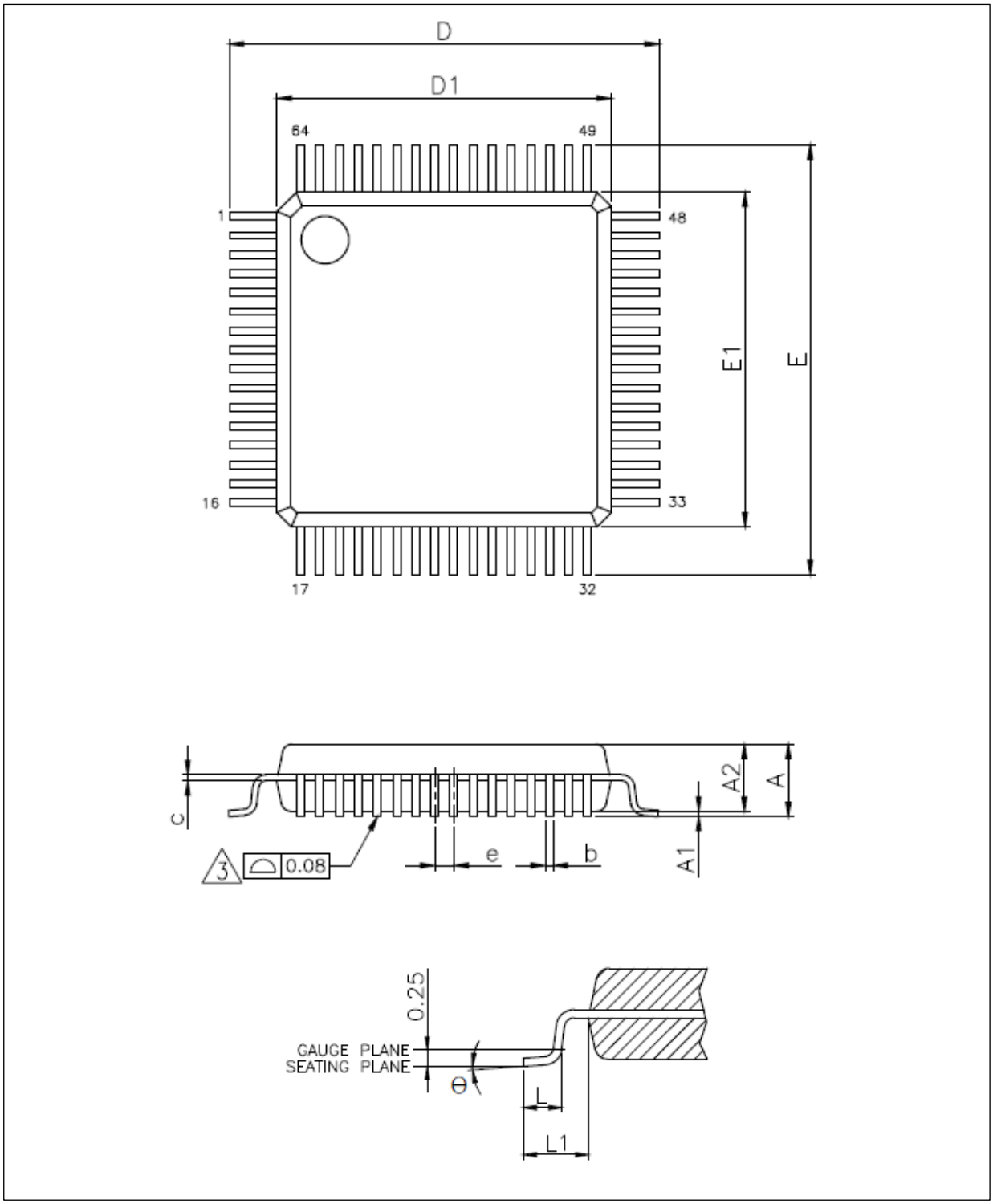


Table 56. LQFP64 – 7 x 7 mm 64 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

5.3 LQFP48 – 7 x 7 mm

Figure 32. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline

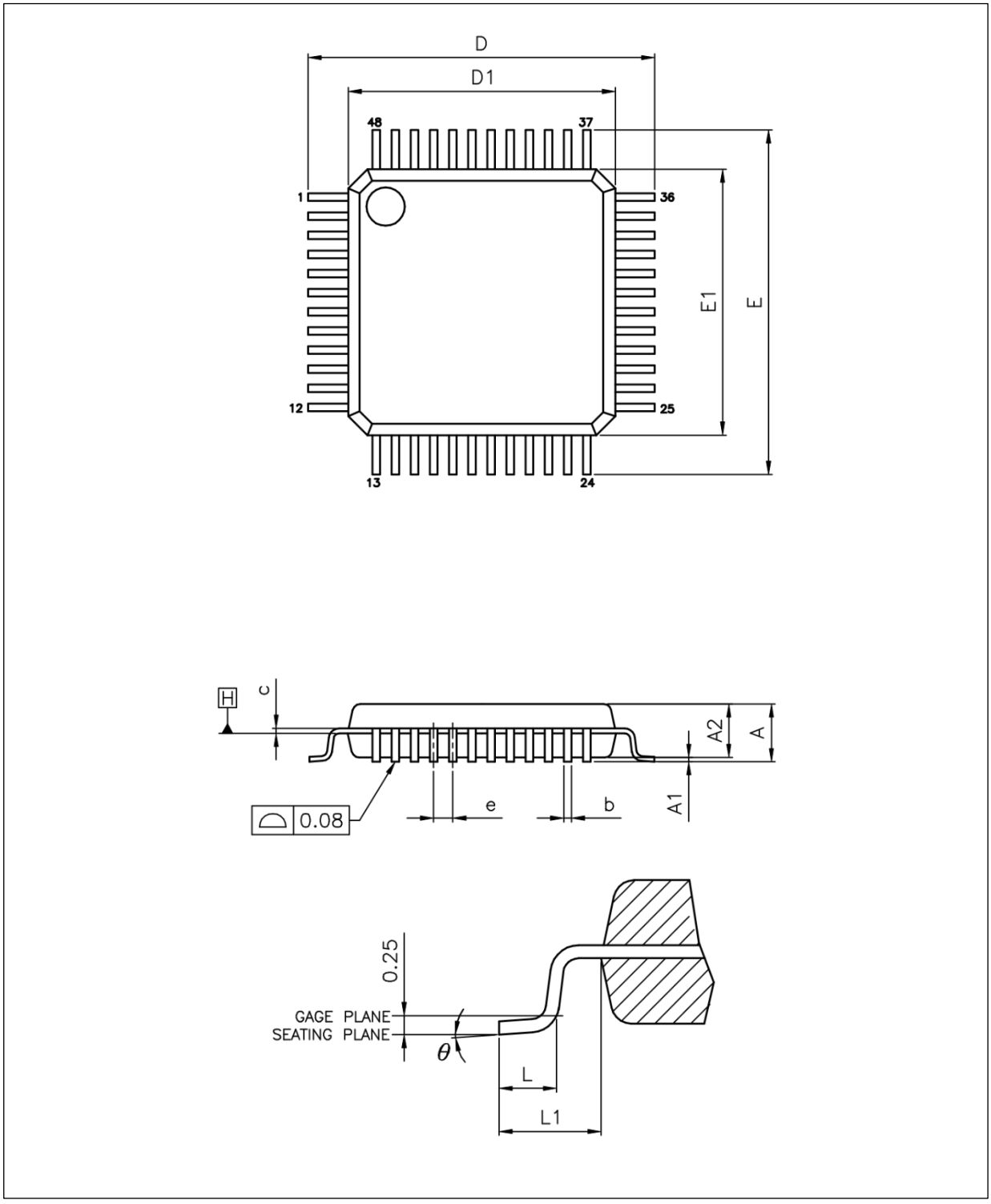


Table 57. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

5.4 QFN48 – 6 x 6 mm

Figure 33. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package outline

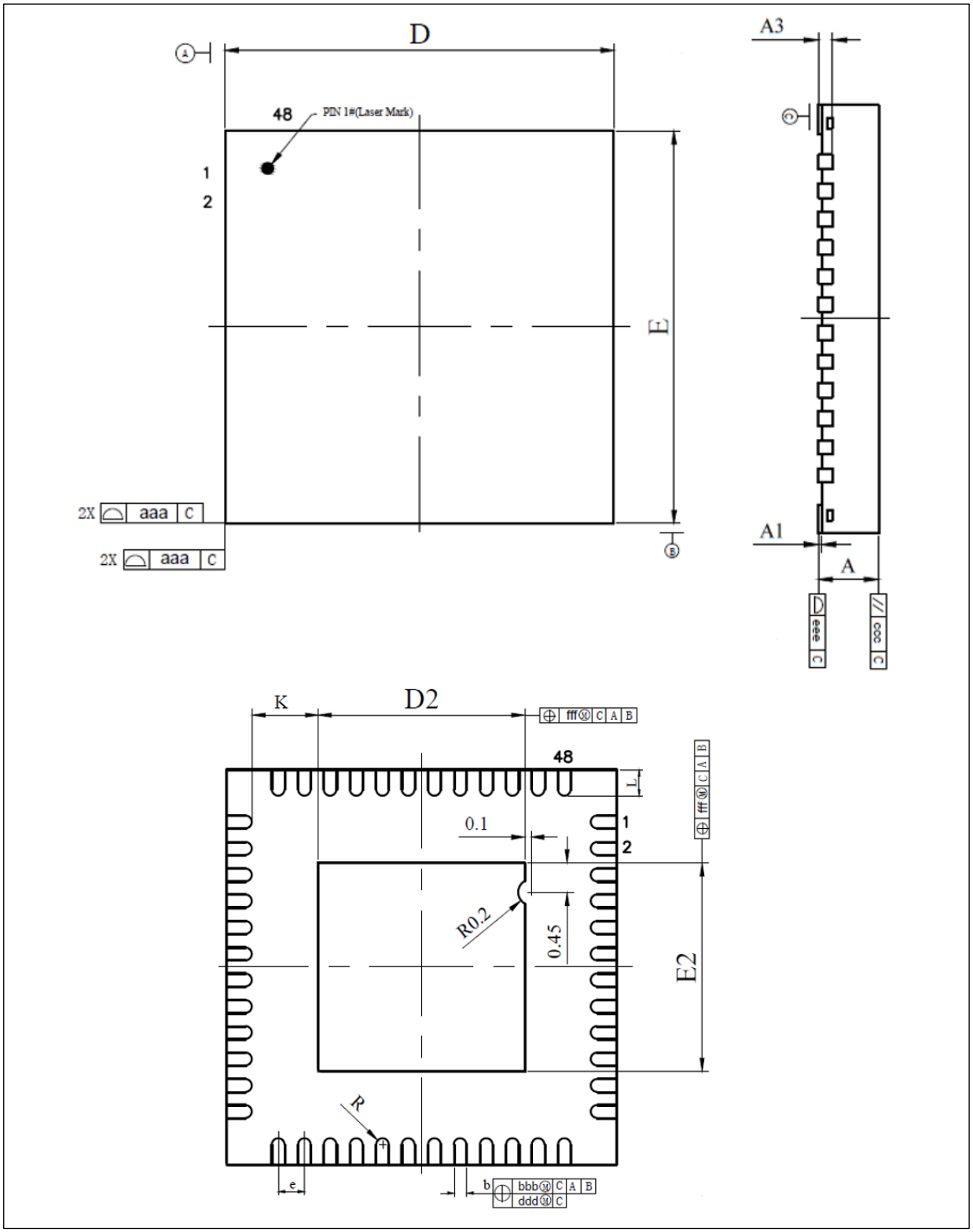


Table 58. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D2	3.07	3.17	3.27
E	5.90	6.00	6.10
E2	3.07	3.17	3.27
e		0.40 BSC.	
K	0.20	-	-
L	0.35	0.40	0.45

5.5 QFN32 – 4 x 4 mm

Figure 34. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package outline

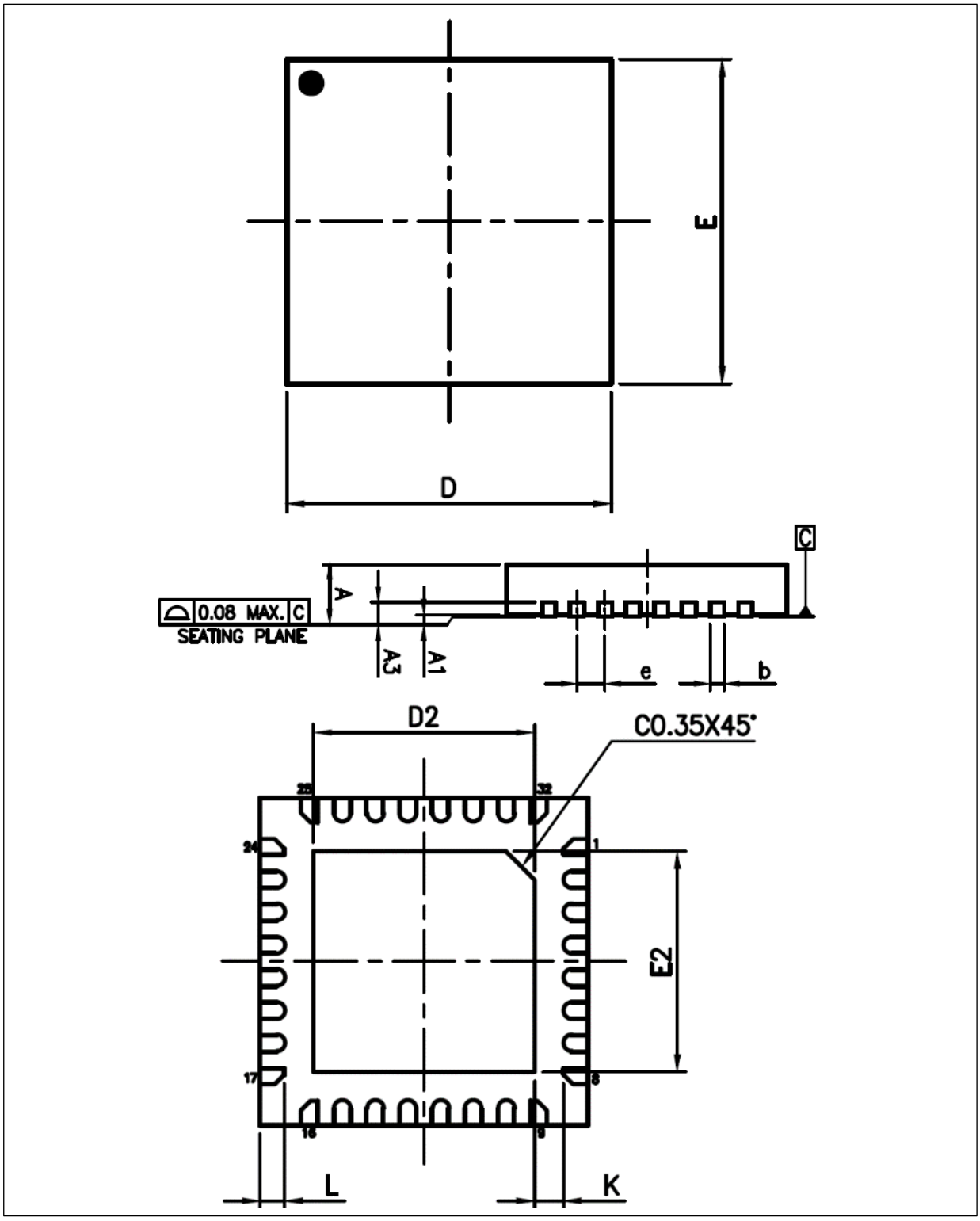


Table 59. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package mechanical data

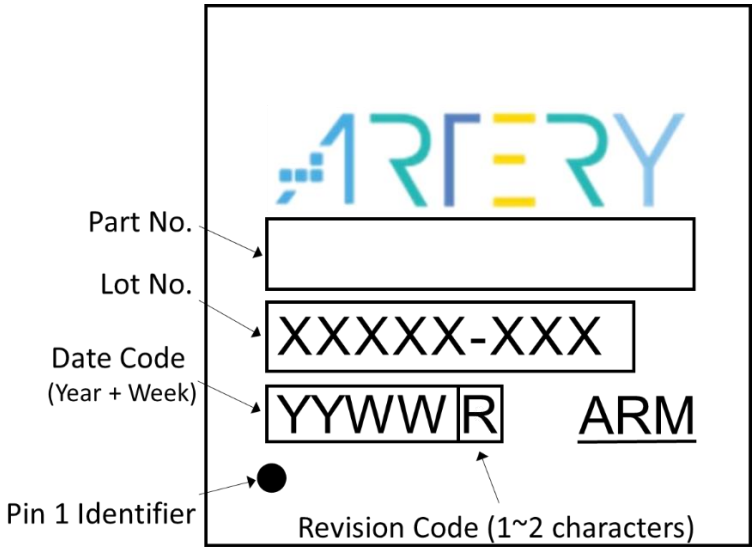
Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e		0.40 BSC.	
K	0.20	-	-
L	0.25	0.30	0.35

5.6 Device marking

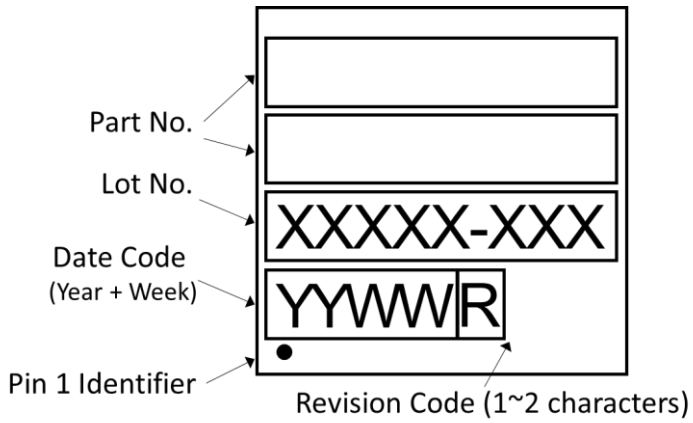
The AT32F405/402 series has two types of packaging labels depending on package types.

Figure 35. Marking example

LQFP64, LQFP48, QFN48



QFN32



(1) Not to scale.

5.7 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material in 1.6 mm thickness. They are guaranteed by design, not tested in production.

Table 60. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient – LQFP64 – 10 x 10 mm	86.0	°C/W
	Thermal resistance junction-ambient – LQFP64 – 7 x 7 mm	94.3	
	Thermal resistance junction-ambient – LQFP48 – 7 x 7 mm	94.3	
	Thermal resistance junction-ambient – QFN48 – 6 x 6 mm	57.1	
	Thermal resistance junction-ambient – QFN32 – 4 x 4 mm	71.5	

6 Part numbering

Table 61. AT32F405/402 series part numbering

Example: AT32 F 4 0 5 R C T 7 -7

Product family

AT32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Core

4 = Cortex®-M4

Product series

0 = Mainstream

Product application

5 = OTGHS + OTGFS series

2 = OTGFS series

Pin count

R = 64 pins

C = 48 pins

K = 32 pins

Internal Flash memory size

C = 256 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package type

T = LQFP

U = QFN

Temperature range

7 = -40 °C to +105 °C

Package information

-7 = LQFP64 - 7 x 7 mm

-4 = QFN32 - 4 x 4 mm

None = other packages

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

7 Revision history

Table 62. Document revision history

Date	Version	Revision note
2023.10.17	2.00	Initial release.
2024.4.1	2.01	1. Modified PA11 and PA12 to support 5 V-tolerant characteristics. 2. Modified the maximum communication rate of USART/UART.

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