

AN0037 Application Note

How to use FPU

Introduction

This application note describes how to use FPU feature on At32 series MCUs.

Applicable products:

	AT32F403
	AT32F403A
Dort ourshor	AT32F407
Fait number	AT32F413
	AT32F435
	AT32F437



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1 Necessary preparations

1.1 Enable FPU in the program

Open the **system_at32f4xx.c** file and find the **void SystemInit** (void) function to confirm that the FPU is enabled in the core, as shown in the black italics in Figure 1.

Note: It is necessary to enable FPU in the program. If the FPU is only set in Keil or IAR but not enabled in the program, the hardfault will happen.

Figure 1. Enable FPU in the program void SystemInit (void) { #if defined (___FPU_USED) && (___FPU_USED == 1U) SCB->CPACR |= ((3U << 10U * 2U) | /* set cp10 full access */ (3U << 11U * 2U)); /* set cp11 full access */ #endif /* reset the crm clock configuration to the default reset state(for debug purpose) */ /* set hicken bit */ CRM->ctrl_bit.hicken = TRUE; /* wait hick stable */ while(CRM->ctrl_bit.hickstbl != SET); /* hick used as system clock */ CRM->cfg_bit.sclksel = CRM_SCLK_HICK; /* wait sclk switch status */ while(CRM->cfg_bit.sclksts != CRM_SCLK_HICK);

2 Set FPU in Keil

2.1 Enable FPU

Options for Target->Target->Floating Point Hardware->Use Single Precision

Device	Target	Output List	ing Vser	C/C++ A	lsm []	Linker	Debug Vtil	ities	
ArteryTek	: AT32F40	3ZC			C-d- (
			Xtal (MHz): 1	2.0	ARM	Compiler:	Use default	compiler versi	on 👻
Operating	g system:	None	-	-			,		
System V	liewer File:	;			ΠU	se Cross-I	Module Optimiza	ation	
AT32F4	03Zx.svd				V 🗸	se MicroL	IB Í	Big Endian	
Use	Custom Fi	le			Floati	ng Point H	lardware:	Use Single Pre	ecision 💌
Read/	Only Mem	ory Areas ——			-Read/	Write Men	nory Areas		
default	off-chip	Start	Size	Startup	default	off-chip	Start	Size	Nolnit
	ROM1:			0		RAM1:			
	ROM2:			0		RAM2:			
	ROM3:					RAM3:			
	on-chip					on-chip			
	IROM1:	0x8000000	0×40000	۰	◄	IRAM1:	0x20000000	0x38000	
	IROM2:			0		IRAM2:			
			02	1 6	1	Dev	e] + [¥-1-

Figure 2. Enable FPU in Keil





2.2 Disable FPU

Options for Target->Target->Floating Point Hardware->Not Used

Device Target Output Listing User C/C++ A	usm Linker Debug Utilities
ArteryTek AT32F403ZC Xtal (MHz): 12.0	Code Generation ARM Compiler: Use default compiler version
System Viewer File: AT32F403Zx.svd	Use Cross-Module Optimization Use MicroLIB Big Endian Floating Point Hardware: Not Used
Read/Only Memory Areas default off-chip Start Size Startup	Read/Write Memory Areas default off-chip Start Size NoInit
ROM1: 0	
	□ RAM3: □ □
on-chip IROM1: 0x8000000 0x40000 (•	on-chip IRAM1: 0x20000000 0x38000
□ IROM2: 0	

Figure 3. Disable FPU in Keil



3 Set FPU in IAR

3.1 Enable FPU

Options ->General Options->FPU->VFPv4 single precision

Category: General Options Static Analysis Runtime Checking C/C++ Compiler Assembler Output Converter Custom Build Build Actions Linker Debugger Simulator CADI CMSIS DAP GDB Server I-jet/JTAGjet J-Link/J-Trace TI Stellaris Nu-Link PE micro ST-LINK	Library Opt Target Outp Processor v © Core © Device © CMSIS-Pa Endian mode © Little © Big © BE32 © BE8	ions 2 ut Libre ariant Cortex Artery ck None Flos FPU D Add Ø DS	MISRA-C:2004 ary Configuration -M4 - Tek AT32F403AVGT7 - sting point setting 16 - lvanced SIMD (NEON) P Extension True	MISRA-C: 1998 Library Options 1
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Figure 4. Enable FPU in IAR



3.2 Disable FPU

Options ->General Options->FPU->None

Options for node "Templat	· · · · · · · · · · · · · · · · · · ·
General Options Static Analysis Runtime Checking C/C++ Compiler Assembler Output Converter Custom Build Build Actions Linker Debugger Simulator CADI CMSIS DAP GDB Server I-jet/JTAGjet J-Link/J-Trace TI Stellaris Nu-Link PE micro ST-LINK Third-Party Driver TI MSP-FET TI XDS	Library Options 2 MISRA-C: 2004 MISRA-C: 1998 Target Output Library Configuration Library Options 1 Processor variant Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 © Device ArteryTek AT32F403AVGT7 Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 © Device ArteryTek AT32F403AVGT7 Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 © Device ArteryTek AT32F403AVGT7 Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 © Device ArteryTek AT32F403AVGT7 Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 © Device ArteryTek AT32F403AVGT7 Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 © CMSIS-Pack None Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 Image: Device Floating point settings Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 Image: Device FPU Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 Image: Device FPU Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4 Image: Cortex-M4<

Figure 5. Disable FPU in IAR



4 Revision history

Date	Version	Revision note
2021.09.18	2.0.0	Initial release

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