AN0029
Application Note

Memory read and write while CPU executing

Introduction

This application note describes how to utilize the zero-wait area in the AT32 MCU memory to guarantee normal CPU execution in the process of erase or programming operation.

Applicable products are listed as follows:

MCU	AT32F403xx
	AT32F413xx
	AT32F403Axx
	AT32F407xx
	AT32F435xx
	AT32F437xx

Contents

List of tables

List of figures

1 Overview

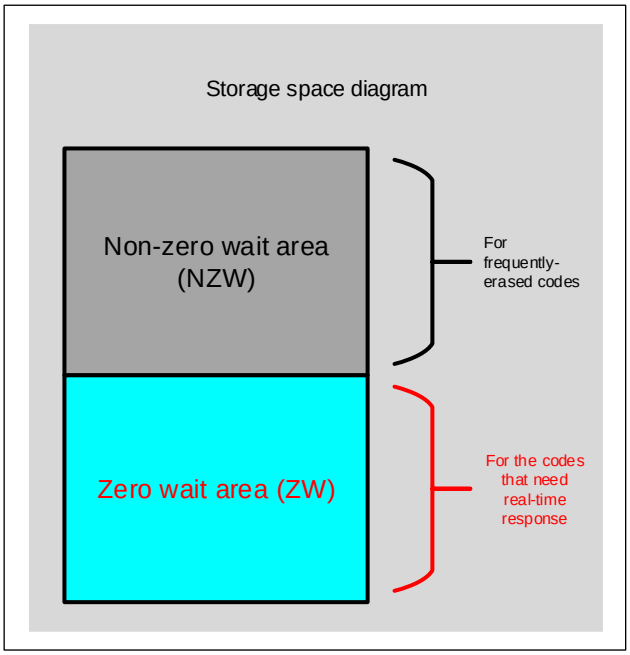
Some applications have strict real-time response requirements, which requireS that the program can still run and respond to the key information during the operations of Flash erase and programming. Usually, the CPU execution would suspend for a long time when performing erase operation, which may lead to some abnormal situations.

The AT32 MUCs with zero wait area (ZW) can be set to place important codes that cannot be stalled in the ZW area, and the frequently-used contents in the NZW area so that the real-time response function can be realized by means of simultaneously executing erase in the NZW and reading in the ZW.

2 Memory architecture

AT32 MCUs internal memory are divided into two parts: zero wait (ZW) area and non-zero wait area (NZW). The user can place the relevant codes in the corresponding area according to their needs.

Figure 1. FLASH memory space



3 How to erase and read simultaneously

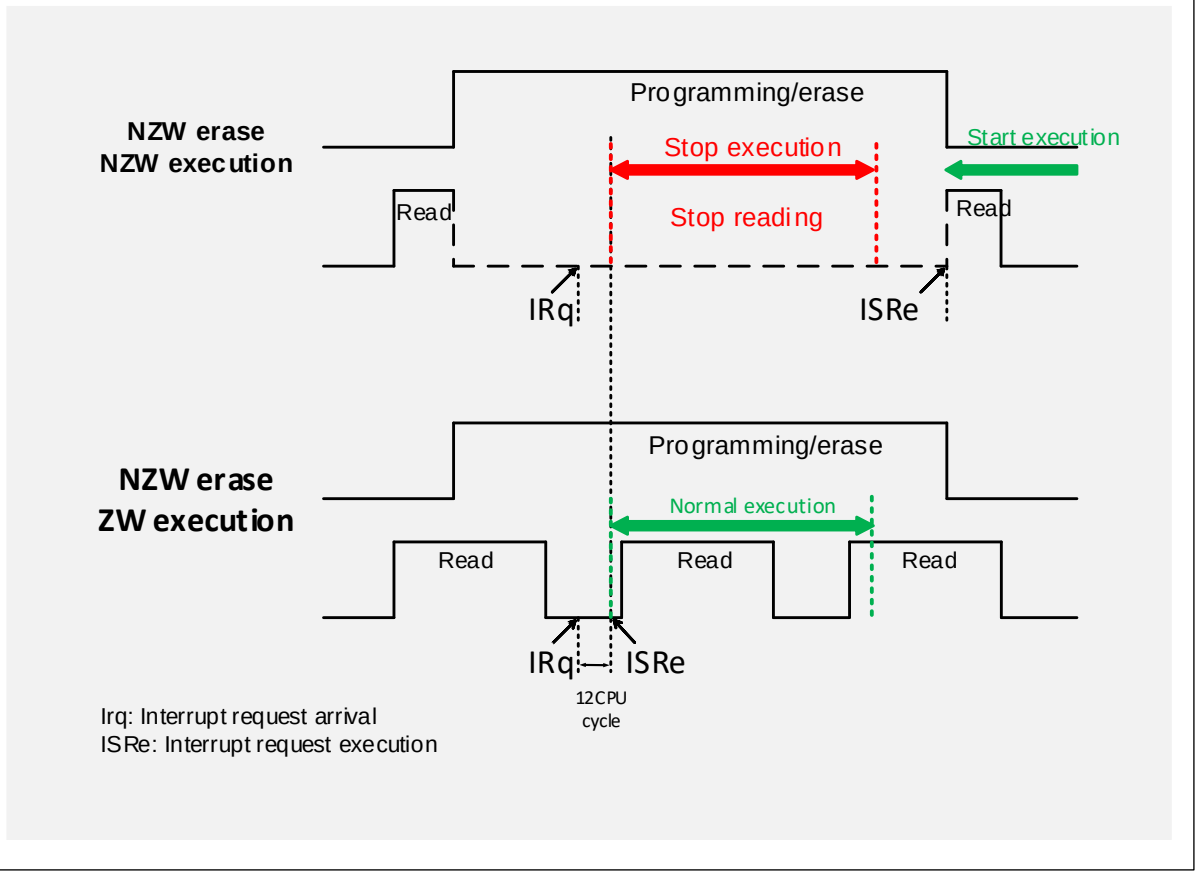
Important codes (such as interrupt processing functions) in the program need to be normally responded when performing erase operation. This section gives an example to explain how to implement this function. The table below describes the possibility of execution between the two memory areas.

Table 1. NZW and ZW

	Non-zero wait area (NZW)		
	Read	Programming	Erase
Zero wait (ZW) read	Not allowed	Allowed	Allowed

When performing Flash erase in NZW area, the codes in the ZW area can be executed normally, and interrupt processing can also be responded in time, as shown in the figure 2.

Figure 2. Erase and read execution



For example:

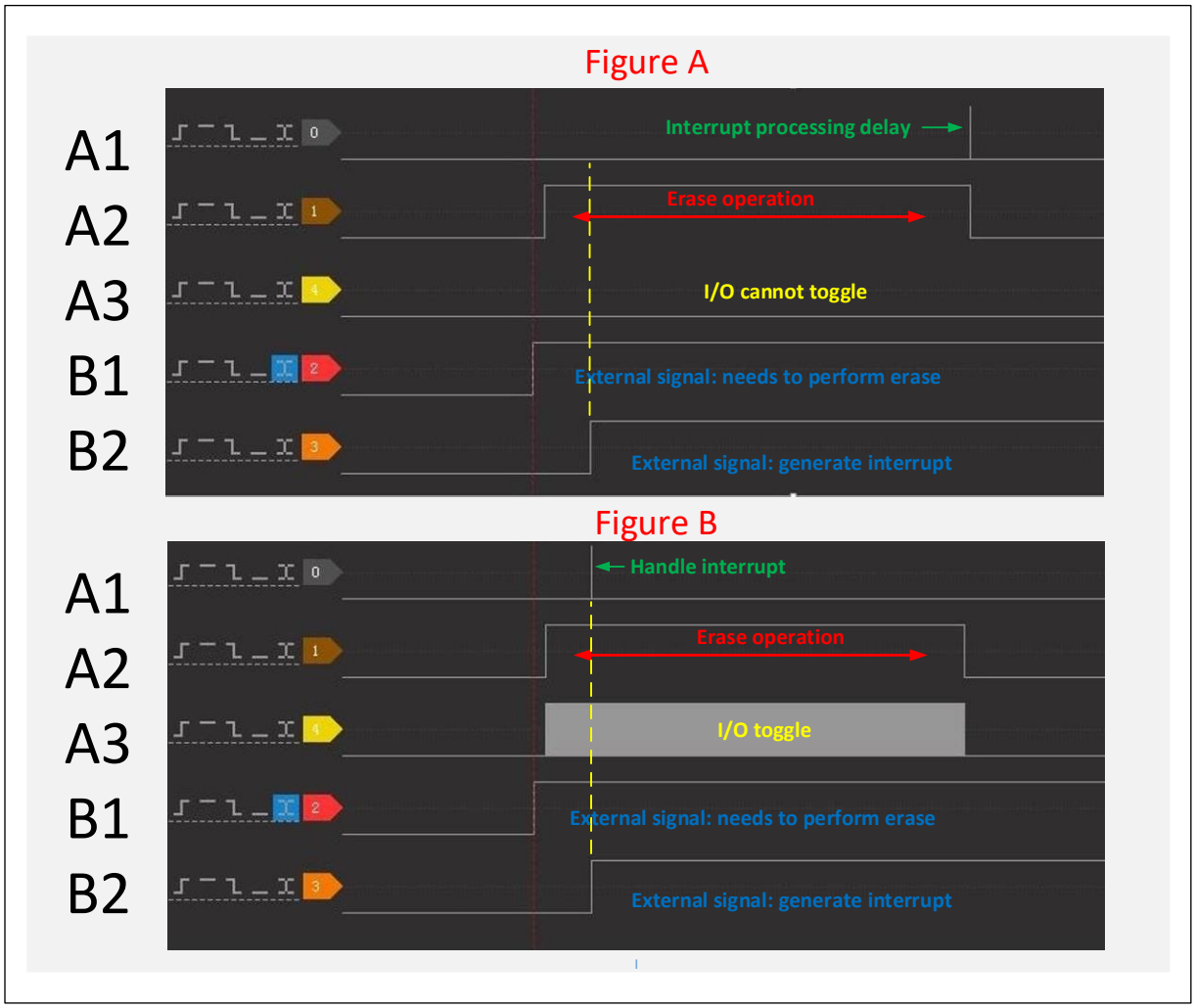
Two AT32F403 evaluation boards are used in this test. The board A is used to demonstrate the code execution when erasing, and the board B is used to generate signals to trigger A to start demonstration.

1. Three I/O signals are set on the board A. The A1 will toggle once after entering external interrupt, A2 before and after sector erase, and A3 during the sector erase.

2. The board B generates the B1 and B2 signals. Set B1 as high, and then B2 high after a delay of 5ms.
3. When detecting a high level on B1, the board A waits for 1ms to start performing one sector erase operation, with the B2 signal connected to the external interrupt of A.

- Figure A: The board A program is running in NZW area, erasing the sector in the NZW area (address 0x08008000). The A1 external interrupt enters only after the erase operation is completed, and A3 I/O cannot toggle during the erase operation (CPU stall program is held).
- Figure B: The board A program is running in the ZW area, erasing the sector in the NZW area (address 0x08008000). The A1 external interrupt is processed normally during the erase operation, and the A3 I/O can toggle, too.

Figure 3. Logic analyzer demonstration diagram



4 Demo code

The AT32F403A evaluation board is used in this demo code. The procedure is as follows:

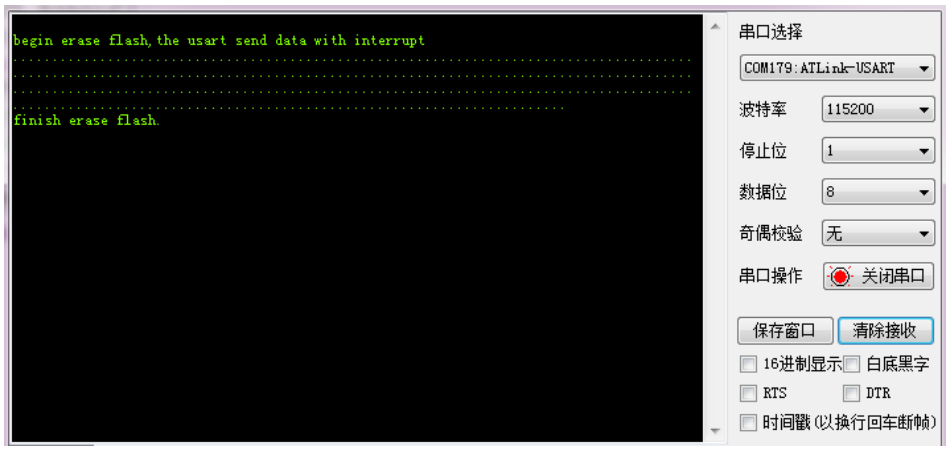
1. Press “USER” button on the board to perform Flash page erase.
2. USART sends data with interrupt during page erase.
3. Verify if the program is executed correctly by checking if the serial interface can print the data during erase.

There are two project targets in the program. Through macro definition, the **executable_project** puts the serial interface interrupt processing functions in the ZW area, while the **hold_project** put them in the NZW area, as shown in the below figure.

```
#ifndef EXECUTABLE
void USART1_IRQHandler(void) __attribute__((section(".ARM.__at_0x08040000")));
#endif
```

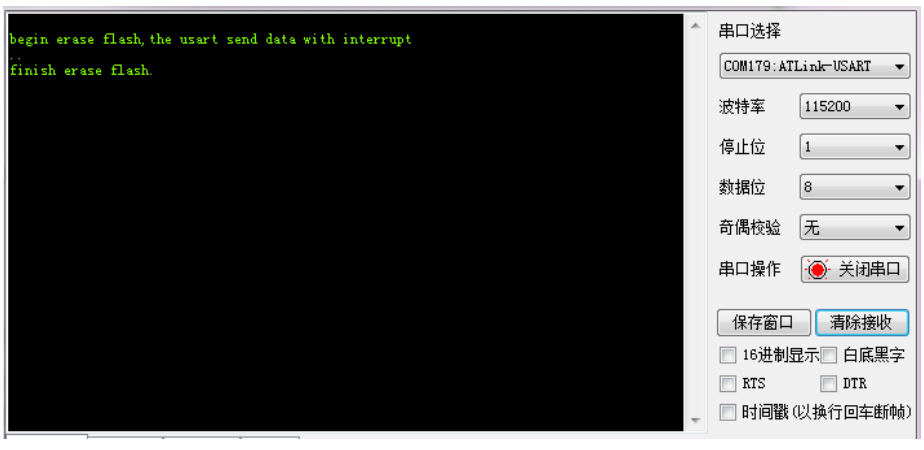
executable_project:

USART interrupt can enter and send data normally during erase:



hold_project:

During erase, USART interrupt cannot enter or send data, as shown below (the two data in the figure are sent during the period between USART interrupt and the writing of CTRL_STRT_Set bit into the Flash CTRL register)



5 Revision history

Table 2. Document revision history

Date	Revision	Changes
2020.01.17	2.0.0	Initial release

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Purchasers are solely responsible for the selection and use of ARTERY's products and services, and ARTERY assumes no liability whatsoever relating to the choice, selection or use of the ARTERY products and services described herein.

No license, express or implied, to any intellectual property rights is granted under this document. If any part of this document deals with any third party products or services, it shall not be deemed a license grant by ARTERY for the use of such third party products or services, or any intellectual property contained therein, or considered as a warranty regarding the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

Unless otherwise specified in ARTERY's terms and conditions of sale, ARTERY provides no warranties, express or implied, regarding the use and/or sale of ARTERY products, including but not limited to any implied warranties of merchantability, fitness for a particular purpose (and their equivalents under the laws of any jurisdiction), or infringement of any patent, copyright or other intellectual property right.

Purchasers hereby agrees that ARTERY's products are not designed or authorized for use in: (A) any application with special requirements of safety such as life support and active implantable device, or system with functional safety requirements; (B) any air craft application; (C) any automotive application or environment; (D) any space application or environment, and/or (E) any weapon application. Purchasers' unauthorized use of them in the aforementioned applications, even if with a written notice, is solely at purchasers' risk, and is solely responsible for meeting all legal and regulatory requirement in such use.

Resale of ARTERY products with provisions different from the statements and/or technical features stated in this document shall immediately void any warranty grant by ARTERY for ARTERY products or services described herein and shall not create or expand in any manner whatsoever, any liability of ARTERY.