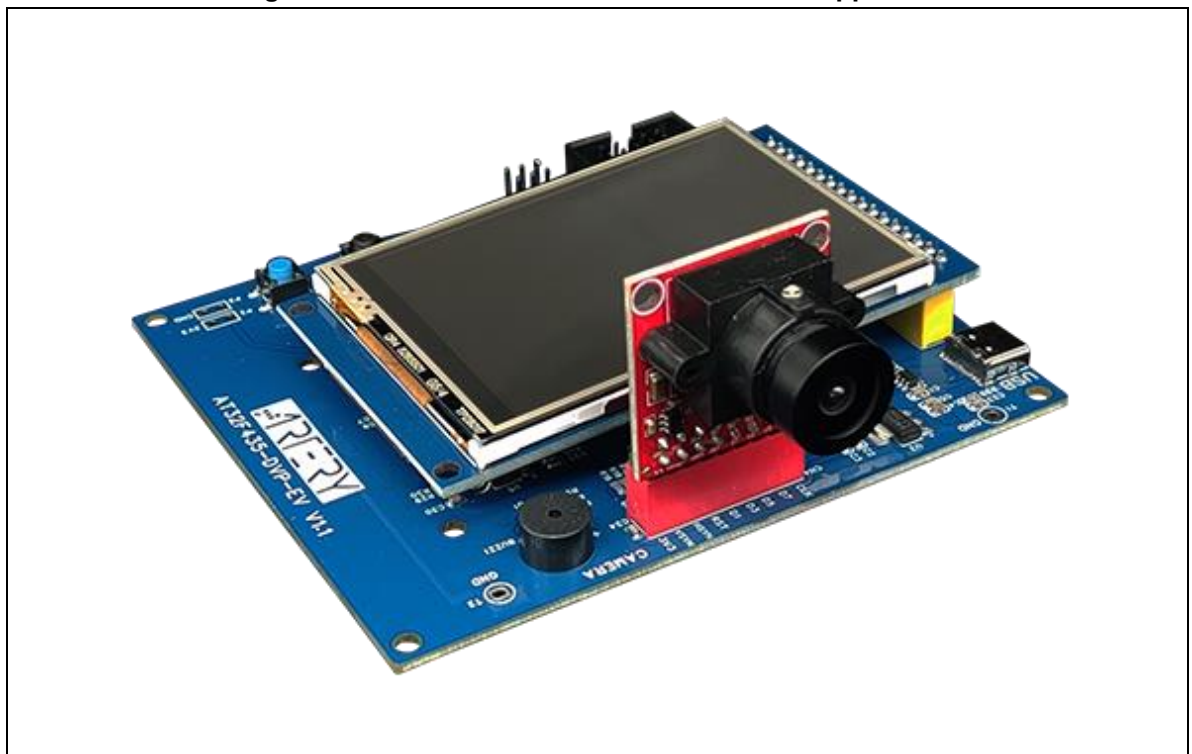


Introduction

AT32F435-DVP-EV evaluation board is designed to help you accelerate your design and development in video application solutions.

AT32F435-DVP-EV is an evaluation board based on the AT32F435VMT7 microcontroller. The evaluation board can be connected to the digital camera module, large-capacity SDRAM, QSPI PSRAM, 2.8-inch TFT-LCD panel and buzzer. It also gets connected with a PC for data transfer via a USB interface.

Figure 1. AT32F435-DVP-EV evaluation board appearance



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1 Overview

1.1 Features

AT32F435-DVP-EV has the following features:

- ARM®Cortex®-M4 core-based 32-bit AT32F435VMT7 microcontroller with 4032 KB Flash memory and 384 KB SRAM, in LQFP100 package
- Multiple power-supply options:
 - 5 V and 3V3 pins of AT-Link connector
 - OTGFS2 bus interface (V_{BUS} 5 V) of AT32F435-DVP-EV
- Camera:
 - Digital camera module connector
 - 2.8-inch 320 x 240 TFT-LCD panel (connected to XMC interface) with capacitive touch panel
- Extension memories
 - 32 Mbytes SDRAM (connected to XMC interface)
 - 8 Mbytes SPI PSRAM (connected to QSPI1 interface)
- Clock sources:
 - 8 MHz HEXT crystal
 - 32.768 kHz LEXT crystal
- LEDs:
 - LED1 (red) indicates that 3.3V power of the board is supplied
 - LED2 (yellow) and LED3 (green) indicate operation status
- User interface:
 - 1x User button and 1x Reset button
 - Buzzer
- Communication interfaces:
 - USART2 lead out to the AT-Link connector
 - SPI4 used to control TFT-LCD panel
 - I²C2 used to control camera module
 - OTGFS2 with a USB type-C connector

1.2 Definition of terms

- **Jumper JPx ON**
Jumper fitted
- **Jumper JPx OFF**
Jumper not fitted
- **Resistor Rx ON**
Short by solder or 0 Ω resistor
- **Resistor Rx OFF**
Connections left Open

2 Quick start guide

2.1 Getting started

Configure the AT32F435-DVP-EV board in the following sequence:

1. Plug Camera module into CN4 (digital camera module connector) with lens facing outward
2. Check the Jumpers' position on board:
JP1 is connected to GND or OFF (BOOT0 = 0, and BOOT0 has an internal pull-down resistor in the AT32F435VMT7)
JP2 can be connected to any location when LED2 is not used or put JP2 in floating
3. Connect CN2 to a PC via a USB cable (Type-A to Type-C) so that the board is powered
4. LED1 (red) is always on
5. TFT-LCD displays "ARTERY" figure and then the image captured by digital camera module

2.2 Development toolchains

- ARM® Keil®: MDK-ARM™
- IAR™: EWARM
- AT32 IDE

3 Hardware layout and configuration

The AT32F435-DVP-EV board is designed around AT32F435VMT7 microcontroller in LQFP100 package.

[Figure 2](#) shows the connection between AT32F435VMT7 and peripherals. [Figure 3](#) and [Figure 4](#) show their respective positions on the AT32F435-DVP-EV board.

Figure 2. Hardware block diagram

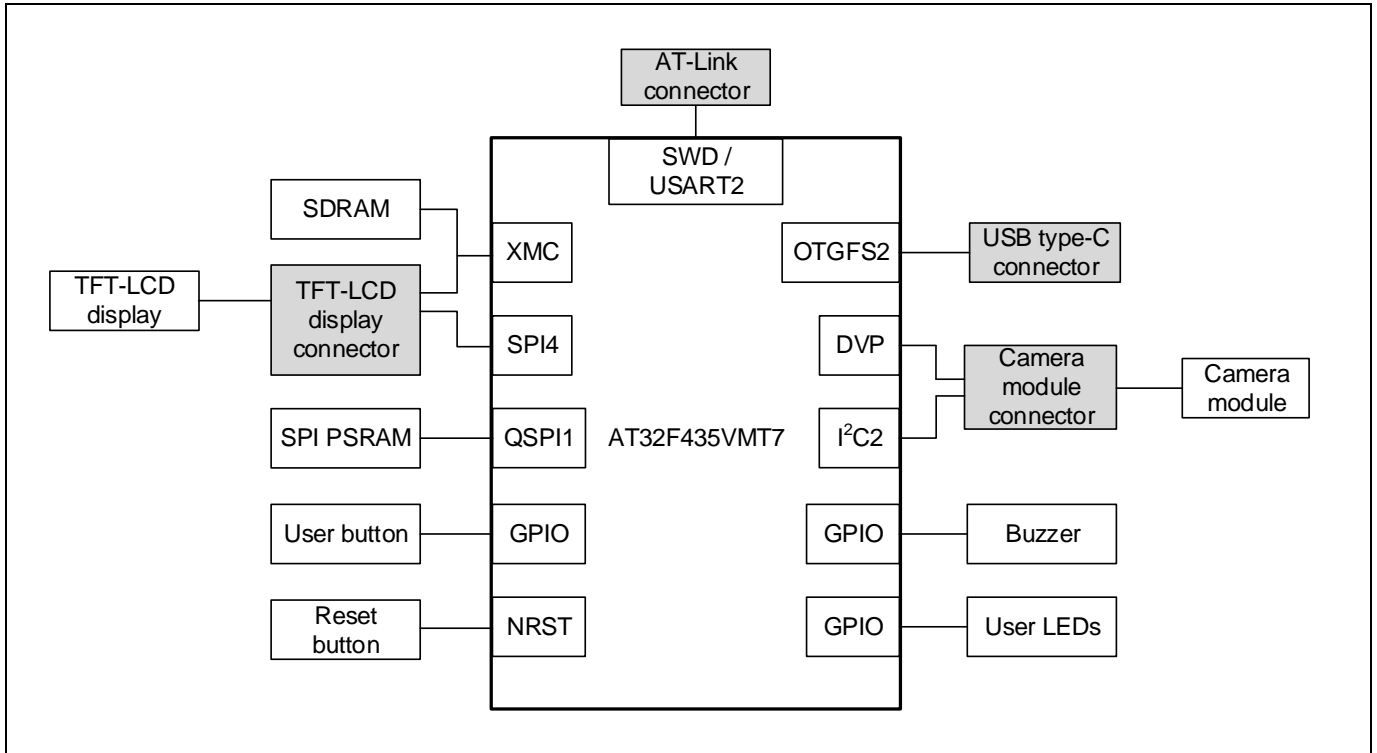


Figure 3. Top layer

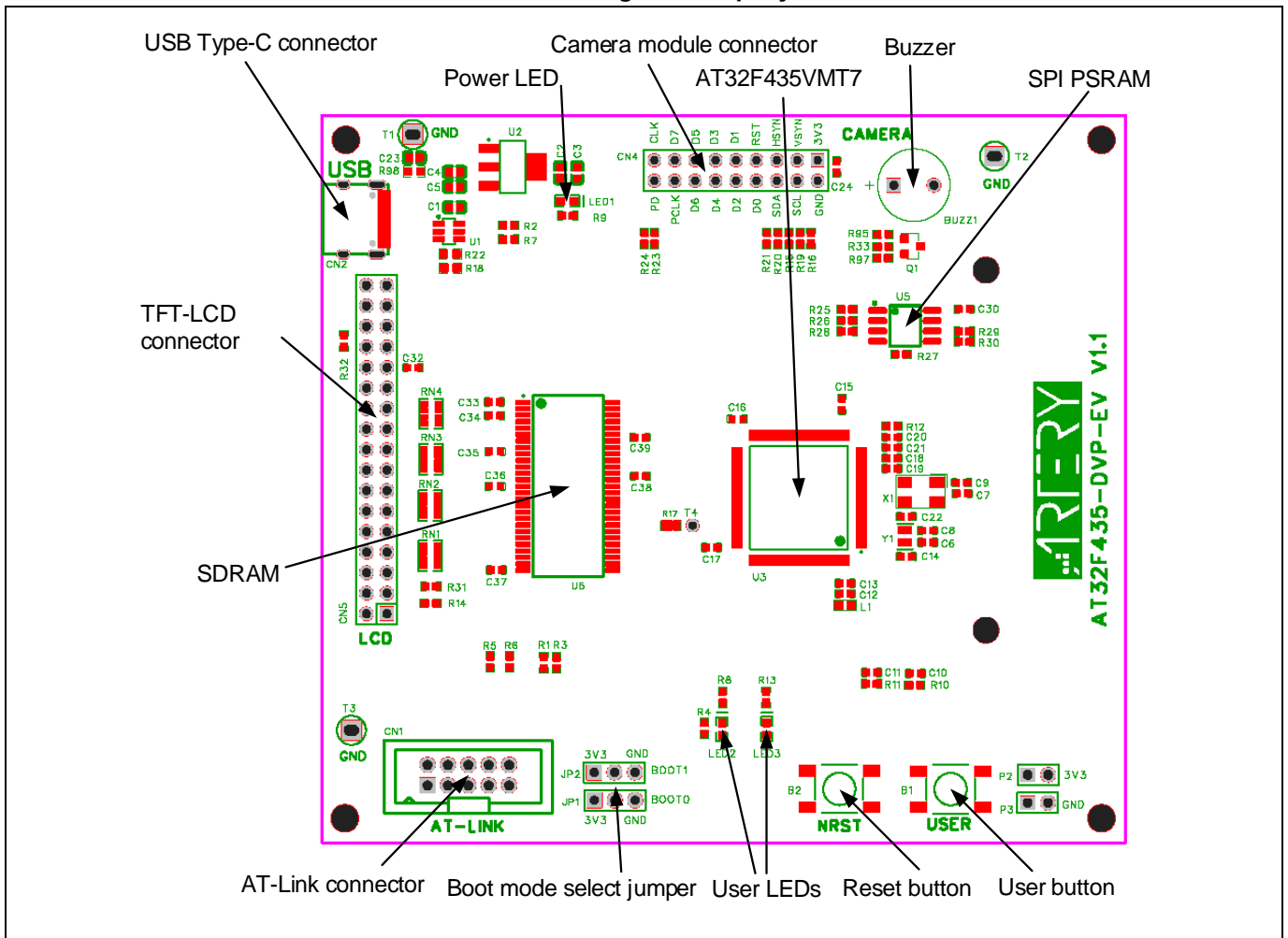
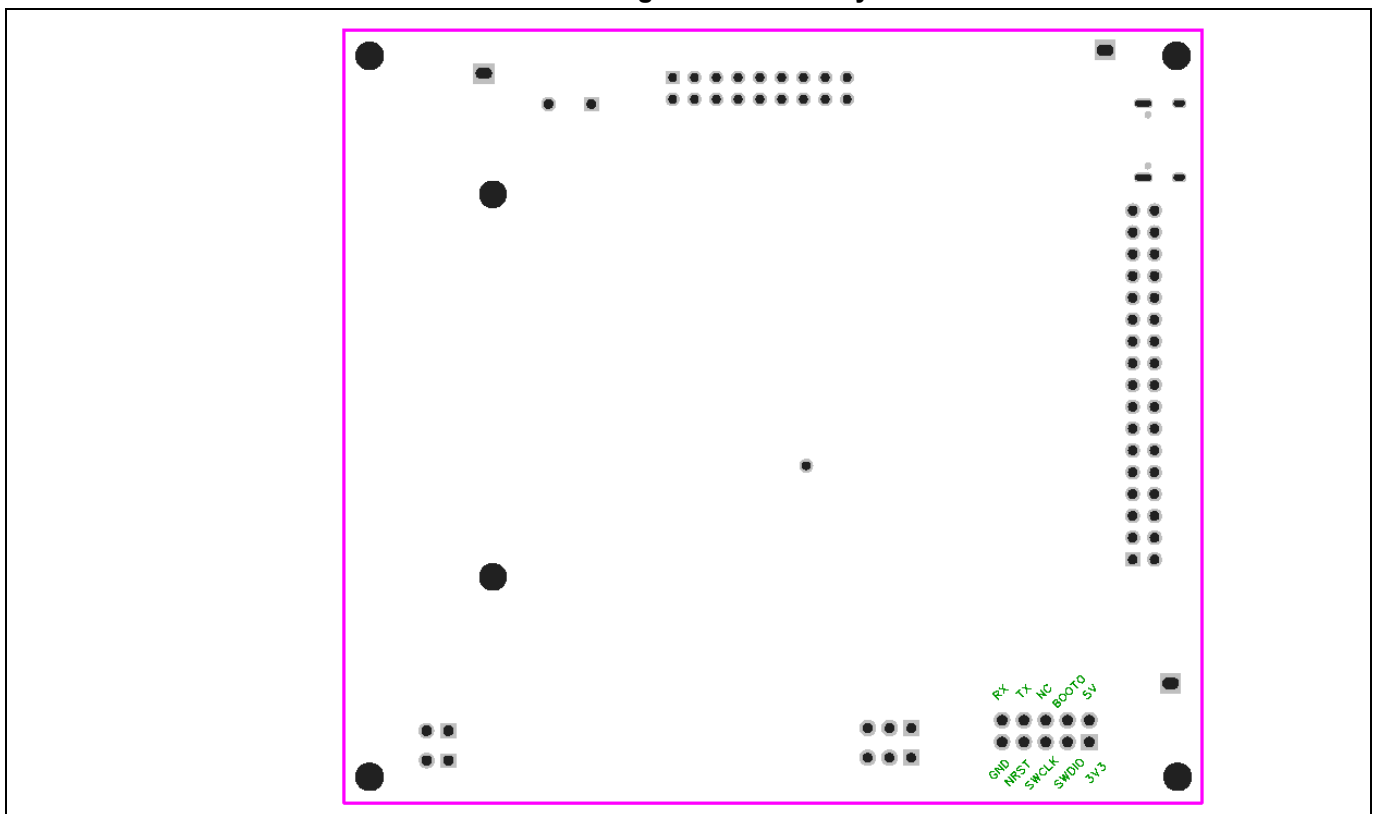


Figure 4. Bottom layer



3.1 Power supply sources

The 5 V power supply source required for AT32F435-DVP-EV board can be from the USB cable or AT-Link connector CN1. Then the 5 V power supply provides the 3.3 V to the microcontroller and peripherals via a power regulator (U2) on board.

The LED1 (red) is always on when the AT32F435-DVP-EV board is being powered.

3.2 Boot mode selection

At startup, the board boots from the following memory locations.

Table 1. Boot mode selection

Jumper	Pin configuration		Description
	BOOT1	BOOT0	
JP1 connected to GND or OFF; JP2 connected to any position or OFF	X	0	Boot from the internal Flash memory (Factory default setting)
JP1 connected to 3V3 JP2 connected to GND	0	1	Boot from the system memory, with ISP function
JP1 connected to 3V3 JP2 connected to 3V3	1	1	Boot from SRAM, for debug purpose

3.3 External clock source

The 8 MHz crystal (X1) on the board is used as HEXT clock source of the AT32F435VMT7. The 32.768 kHz crystal (Y1) on the board is used as its LEXT clock source.

3.4 Digital camera module connector

The camera module is connected to the DVP interface of the AT32F435VMT7 via a CN4. The data width is 8-bit. At the same time, the on-board I²C2 interface is used to control camera module to initialize it and obtain its status.

3.5 TFT-LCD touch panel connector

The 2.8-inch 320 x 240 TFT-LCD capacitive touch panel is connected to CN5 connector, by default. The AT32F435VMT7 board uses the 16-bit XMC parallel interface to transfer video data. TFT-LCD touch signals communicate with the AT32F435VMT7 via a SPI4.

3.6 SDRAM

The on-board 16-bit 32-Mbyte SDRAM (U6, part number W9825G6KH-6) is connected to the AT32F435VMT7 via the XMC interface to extend the program and data memory as well as random access memory. The SDRAM is already available on the LQFP100 package, without having to use larger LQFP144 package.

3.7 SPI PSRAM

The on-board 8-Mbyte SPI PSRAM (U5, part number APS6404L-3SQR) is connected to the AT32F435VMT7 via the QSPI1 interface to serve as an extension of random access memory.

3.8 LEDs

- **Power LED1**

Red color, indicates that the AT32F435-DVP-EV board is being powered.

- **User LED2**

Yellow color, connected to the PB2 pin of AT32F435VMT7.

- **User LED3**

Green color, connected to the PA5 pin of AT32F435VMT7.

3.9 Buttons

- **User button B1**

It is connected to the PA0 of AT32F435VMT7 as a wake-up button.

- **Reset button B2**

It is connected to NRST to reset AT32F435VMT7.

3.10 Buzzer

The buzzer (BUZZ1) can be switched on and off, by using the PE3 of the AT32F435VMT7 to control the triode SS8050 (Q1).

3.11 OTGFS connector

AT32F435-DVP-EV board supports OTGFS2 full-speed/low-speed host mode or full-speed device mode, via a USB type-C connector (CN2). In device mode, AT32F435VMT7 can be directly connected to the host through USB type-C connector, and the V_{BUS} can be used as 5 V input of the AT32F435-DVP-EV board.

3.12 0 Ω resistors

Table 2. 0 Ω resistor settings

Resistors	State ⁽¹⁾	Description
R17	OFF	CLKOUT1 is not connected with CN4 (camera module connector)
	ON	CLKOUT1 is connected with CN4 (camera module connector)

(1) Rx factory default state is shown in **BOLD**.

4 Pin assignment

Each of the GPIOs has its specific function and is connected to one or more external devices to optimize the number of GPIO features available in LQFP100 package. The table below lists the GPIO assignment of the AT32F435VMT7 and their connection with the external devices.

Table 3. AT32F435VMT7 pin assignment

Pin number	Pin name	Function	Connected device 1	Connected device 2
1	PE2	XMC_SDNCAS	W9825G6KH (U6)	-
2	PE3	PE3	Buzzer (BUZZ1)	-
3	PE4	DVP_D4	Camera module connector (CN4)	-
4	PE5	DVP_D6	Camera module connector (CN4)	-
5	PE6	XMC_SDNRAS	W9825G6KH (U6)	-
7	PC13	Unused	-	-
8	PC14	LEXT_IN	32 kHz crystal (Y1)	-
9	PC15	LEXT_OUT	32 kHz crystal (Y1)	-
12	PH0	HEXT_IN	8 MHz crystal (X1)	-
13	PH1	HEXT_OUT	8 MHz crystal (X1)	-
15	PC0	PC0	-	TFT-LCD panel connector (CN5)
16	PC1	PC1	Camera module connector (CN4)	-
17	PC2	XMC_NWE	-	TFT-LCD panel connector (CN5)
18	PC3	PC3	Camera module connector (CN4)	-
23	PA0	PA0	User button (B1)	-
24	PA1	SPI4_MOSI	-	TFT-LCD panel connector (CN5)
25	PA2	USART2_TX	AT-Link connector	-
26	PA3	USART2_RX	AT-Link connector	-
29	PA4	DVP_HSYNC	Camera module connector (CN4)	-
30	PA5	PA5	LED3	-
31	PA6	DVP_PCLK	Camera module connector (CN4)	-
32	PA7	XMC_SDNWE	W9825G6KH (U6)	-
33	PC4	XMC_NE4	-	TFT-LCD panel connector (CN5)
34	PC5	XMC_NOE	-	TFT-LCD panel connector (CN5)
35	PB0	QSPI1_IO0	APS6404L-3SQR (U5)	-
36	PB1	QSPI1_SCK	APS6404L-3SQR (U5)	-

Pin number	Pin name	Function	Connected device 1	Connected device 2
37	PB2 / BOOT1	PB2 / BOOT1	LED2	-
38	PE7	XMC_D4	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
39	PE8	XMC_D5	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
40	PE9	XMC_D6	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
41	PE10	XMC_D7	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
42	PE11	XMC_D8	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
43	PE12	XMC_D9	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
44	PE13	XMC_D10	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
45	PE14	XMC_D11	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
46	PE15	XMC_D12	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
47	PB10	QSPI1_CS	APS6404L-3SQR (U5)	-
48	PB11	EXINT11	-	TFT-LCD panel connector (CN5)
49	PH3	I2C2_SDA	Camera module connector (CN4)	-
51	PB12	SPI4_CS	-	TFT-LCD panel connector (CN5)
52	PB13	SPI4_SCK	-	TFT-LCD panel connector (CN5)
53	PB14	OTGFS2_D-	OTGFS2 connector (CN2)	-
54	PB15	OTGFS2_D+	OTGFS2 connector (CN2)	-
55	PD8	XMC_D13	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
56	PD9	XMC_D14	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
57	PD10	XMC_D15	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
58	PD11	XMC_SDBA0	W9825G6KH (U6)	-
59	PD12	XMC_SDBA1	W9825G6KH (U6)	-
60	PD13	XMC_SDCLK	W9825G6KH (U6)	-
61	PD14	XMC_D0	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
62	PD15	XMC_D1	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
63	PC6	XMC_A0	W9825G6KH (U6)	-
64	PC7	XMC_A1	W9825G6KH (U6)	-
65	PC8	XMC_A2	W9825G6KH (U6)	-
66	PC9	XMC_A3	W9825G6KH (U6)	-
67	PA8	XMC_A4 / CLKOUT1	W9825G6KH (U6)	Camera module connector (CN4)

Pin number	Pin name	Function	Connected device 1	Connected device 2
68	PA9	DVP_D0	Camera module connector (CN4)	-
69	PA10	DVP_D1	Camera module connector (CN4)	-
70	PA11	DVP_D2	Camera module connector (CN4)	-
71	PA12	DVP_D3	Camera module connector (CN4)	-
72	PA13	SWDIO	AT-Link connector	-
73	PH2	I2C2_SCL	Camera module connector (CN4)	-
76	PA14	SWCLK	AT-Link connector	-
77	PA15	QSPI1_IO2	APS6404L-3SQR (U5)	-
78	PC10	QSPI1_IO1	APS6404L-3SQR (U5)	-
79	PC11	XMC_D2	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
80	PC12	XMC_D3	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
81	PD0	XMC_A5	W9825G6KH (U6)	-
82	PD1	XMC_A6	W9825G6KH (U6)	-
83	PD2	XMC_A7	W9825G6KH (U6)	-
84	PD3	XMC_A8	W9825G6KH (U6)	-
85	PD4	XMC_A9	W9825G6KH (U6)	-
86	PD5	XMC_A10	W9825G6KH (U6)	TFT-LCD panel connector (CN5)
87	PD6	XMC_A11	W9825G6KH (U6)	-
88	PD7	XMC_A12	W9825G6KH (U6)	-
89	PB3	QSPI1_IO3	APS6404L-3SQR (U5)	-
90	PB4	DVP_D5	Camera module connector (CN4)	-
91	PB5	XMC_SDCKE1	W9825G6KH (U6)	-
92	PB6	XMC_SDCS1	W9825G6KH (U6)	-
93	PB7	DVP_VSYNC	Camera module connector (CN4)	-
95	PB8	SPI4_MISO	-	TFT-LCD panel connector (CN5)
96	PB9	DVP_D7	Camera module connector (CN4)	-
97	PE0	XMC_SDDQML	W9825G6KH (U6)	-
98	PE1	XMC_SDDQMH	W9825G6KH (U6)	-

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
2021.12.17	1.00	Initial release
2023.12.4	1.10	1. Replaced CN2 with USB type-C 2. Replaced U5 with APS6404L-3SQR-SN 3. Optimized PCB routing

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